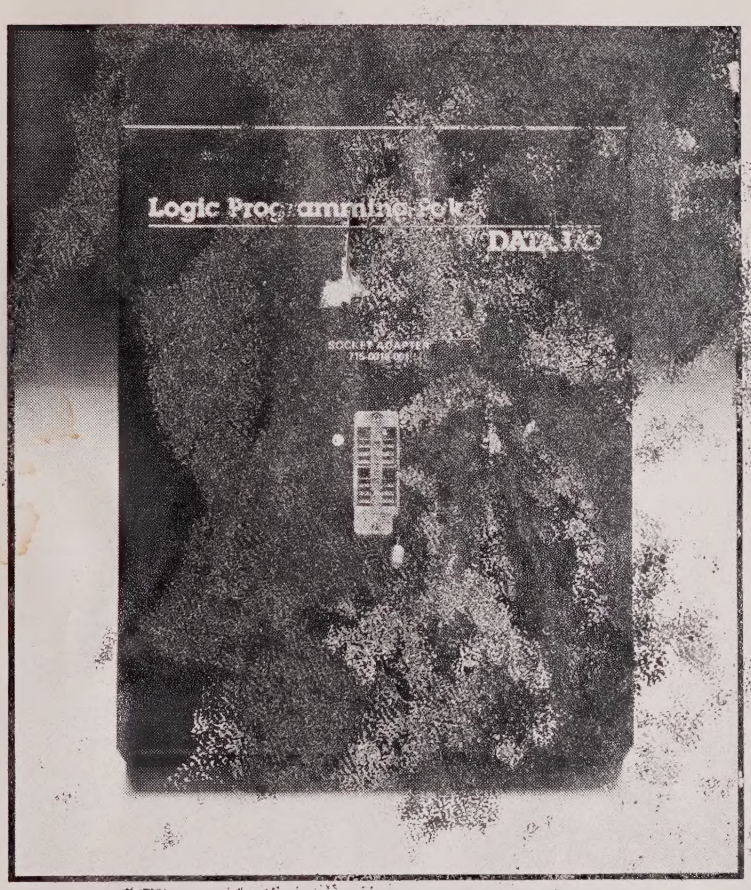
DATA I/O



SIGNETICS INTERACTIVE IFL LOGIC PROGRAMMING PAK 950-0104

10-950-0104-001 REV B FEB 82

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SECTION 1
INTRODUCTION

1.1 APPLICATIONS

The Signetics Interactive IFL Logic Programming Pak adapts Data I/O programmers to program and read Signetics Series 28 and Series 20 Integrated Fused Logic (IFL) devices. A socket adapter is used to configure the programming module for specific devices within these families. These devices are the Field Programmable Gate Array (FPGA), the Field Programmable Logic Array (FPLA), the Field Programmable ROM Patch (FPRP), and the Field Programmable Logic Sequencer (FPLS). Table 1-1 lists these parts and the socket adapter necessary for each one. New applications are developed periodically, so consult the latest Data I/O *Comparison Chart of Programmable Devices* for new devices.

Table 1-1. Programming Module Applications

PART NUMBER	OUTPUT TYPE	PIN COUNT	SOCKET ADAPTER
SIGNETICS			
FPLA 82S100	TS	28	715-1594-1
FPLA 82S101	OC	28	715-1594-1
FPGA 82S102	OC	28	715-1595
FPGA 82S103	TS	28	715-1595
FPLS 82S104	OC	28	715-1594-2
FPLS 82S105	TS	28	715-1594-2
FPRP 82S106	OC	28	715-1594-1
FPRP 82S107	TS	28	715-1594-1
FPLA 82S152	OC	20	715-0018-001
FPLA 82S153	TS	20	715-0018-001

TS = tri-state, OC = open collector

1.2 INTERACTIVE LOGIC ENTRY

The Logic Pak uses an interactive process to load your function (truth) table into the programmer's data RAM. With the Logic Pak installed in the programmer, you enter the logic states to the Logic Pak. Each state is represented by one of a set of six characters. The Logic Pak translates these states into data bits representing fuse numbers in the programmer data RAM in the correct bit pattern to program the device.

There are four modes for data entry: front panel, CRT terminal, serial I/O, and master device. Table 1-2 shows which data entry modes are compatible with the various programmer configurations.

NOTE

Except as notes in Section 3, Operation, Program and Verify operations are accomplished according to the instructions in your programmer manual.

1.2.1 FRONT PANEL (INTERACTIVE) ENTRY

With a System 19, logic states can be entered directly from the front panel. This is explained in section 3.4.

1.2.2 CRT TERMINAL (INTERACTIVE) ENTRY

In this mode, you enter the logic states at a terminal in response to prompting from the display. Several display and edit functions allow you to manipulate logic entries or change an entire gate or term. This is described in section 3.5.

1.2.3 SERIAL I/O ENTRY

The Logic Pak lets the programmer accept logic information stored on tape or disc. Section 3.6 covers how to input and output logic information.

1.2.4 MASTER DEVICE ENTRY

Data can also be downloaded from a programmed Signetics device of the same type as those to be programmed. See your programmer manual for procedures for loading from a master device.

Table 1-2. Logic Data Entry for Different Programmer Configurations

PROGRAMMER CONFIGURATION	FRONT PANEL DATA ENTRY (E0)	CRT TERMINAL DATA ENTRY (E1)	SERIAL INPUT DATA ENTRY (E2)	DATA ENTRY BY FUSE NUMBER	MASTER DEVICE DATA ENTRY
System 17 Front Panel	NA	NA	yes	NA	yes
System 17 with Terminal	NA	yes	yes	NA	yes
System 19 Front Panel	yes	NA	yes	yes	yes
System 19 with Terminal	NA	yes	yes	NA	yes
29A Front Panel	NA	NA	yes	yes	yes
29A with Terminal	NA	yes	yes	NA	yes
100A Front Panel	NA	NA	yes	yes	yes
100A with Terminal	NA	yes	yes	NA	yes

1.3 THEORY OF OPERATION

With bits in the programmer data RAM arranged in the proper format, you can start a Program operation via the programmer's keyboard or a remote control command. An address code is sent to the device first. The fuses to be burned are chosen by the bits in the programmer data RAM at that address. Each fuse to be programmed at that address is read, a programming pulse applied, and then the fuse is read again to verify that it has opened.

If it is not open, another programming pulse is applied and the fuse is read again. This is repeated until the allowed maximum number of pulses have been applied or the fuse has opened.

Programming and operation errors are detected automatically. Consult the programmer manual for a list of error codes that are displayed with the programmer you are using. Error codes unique to the Logic Pak are described in section 3.8.

CAUTION

The correspondence between locations used in the programmer data RAM to program specific fuses in the devices has been changed in this hardware (950-0104) versus the earlier 919-1542 and 950-0800. If you are loading data in the programmer via the port using a PROM-type data format (hexadecimal for example), you must prepare new paper tapes or data files for use with the 950-0104. Failure to do so will result in improperly programmed devices. If you are using master devices as your data source or are loading data via the port using the logic format, this change is transparent to you.

1.4 SPECIFICATIONS

Table 1-3 lists the physical and environmental specifications of the 950-0104 Logic Programming Pak.

1.5 CALIBRATION

The need for calibration varies with the amount of use. Generally, we suggest calibration whenever the programming yields fall below Signetics' recommended minimums.

The Logic Pak can only be calibrated on a programmer with an address and data display. If you are using it with a System 17, you will have to calibrate it on a System 19, 100A, or 29A Universal Programmer, or send it to a Data I/O Service Center and we will calibrate it for you.

Table 1-3. Specifications

Weight.	1.18 kg (2 lb. 9.5 oz.).
Dimensions.	20.9 cm x 17 cm x 10.5 cm (8.2″ x 6.7″ x 4.2″).
Operating Temperature Range.	0° to 45°C (32° to 113°F).
Storage Temperature Range.	−40° to 70°C (−40° to 158°F).
Humidity.	to 95% noncondensing.

1.6 WARRANTY

Data I/O equipment is warranted against defects in materials and workmanship. The warranty period of 90 days begins when you receive the equipment.

The warranty card inside the back cover of this manual explains the length and conditions of the warranty. For warranty service, contact your nearest Data I/O Service Center.

1.7 SERVICE

Data I/O maintains Service Centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. In addition to repairs, all Data I/O products are calibrated. A list of all Data I/O Service Centers is located in the back of this manual.

1.8 ORDERING

To place an order for equipment, contact your Data I/O sales representative. Orders for shipment must contain the following information:

- Description of the equipment. (See the latest Data I/O Price List or contact your sales representative for equipment and part numbers.)
- Quantity of each item ordered.
- Shipping and billing address of firm, including zip code.
- Name of person ordering equipment.
- Purchase order number.
- Desired method of shipment.

SECTION 2
INSTALLATION

2.1 INSPECTION

The Logic Pak was thoroughly tested and inspected before shipment. For trouble-free operation, verify upon receipt that the equipment is in the best possible condition. The unit was carefully packaged before shipment to prevent any possible damage and should arrive free of any defect and in perfect operating condition. All the equipment listed in Table 1-1 should be present. Carefully inspect it for any damage that may have occurred during transit. If you note any damage, file a claim with the carrier and notify Data I/O. Check the operation only after completing the installation procedures in sections 2.2 through 2.5.

Table 2-1. Required Equipment

Description	Data I/O Part Number	Quantity
Signetics Interactive IFL Logic Pak	950-0104-001	1
Keypad Label	415-1804	1
Display Label	415-1803	1
Instruction Manual	10-950-0104-001	1
Operator's Guide	12-950-0104-001	1

2.2 ASSEMBLY AND DISASSEMBLY

The top cover and card carrier of the programming module normally remain attached, but for calibration they must be detached as shown in Figure 2-1. To reattach, interlock the flanges on the upper edges of the top cover and the card carrier. Then press them together and tighten the captive fasteners.

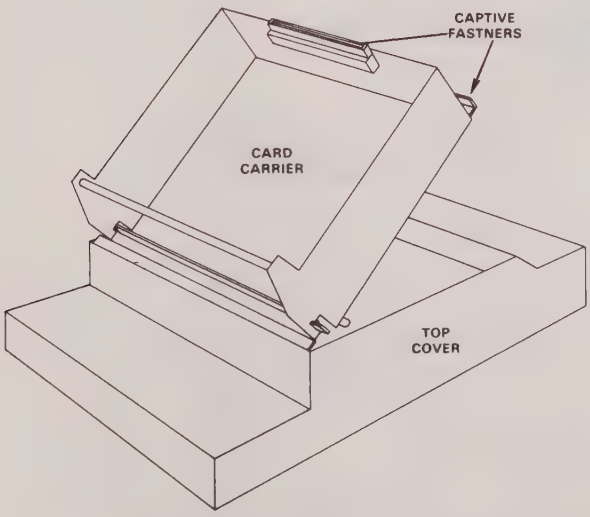


Figure 2-1. Interconnection of the Top Cover and the Card Carrier

2.3 PROGRAMMING MODULE AND SOCKET ADAPTER INSTALLATION

Install the programming module and socket adapters in the programmer according to paragraphs 2.3.1 and 2.3.2.

2.3.1 THE PROGRAMMING MODULE

The programming module can be installed when the programmer power is either on or off. This feature allows the programmer RAM data to remain intact during module changes.

To install the module, slide it into the opening in the programmer, hook the flange of the module under the back edge of the programmer opening, and lower it into position. Press gently on the front edge to insure a good a good connection. If the programmer power is on, the audible beeper will stop when good contact is made. Figure 2-2 illustrates this procedure. Removal is the reverse of installation.

CAUTION

Do not install or remove the module when a device is installed. Voltage transients may cause spurious programming.

2.3.2 THE SOCKET ADAPTER

Install the socket adapter in the receptacle on the front panel of the programming module as shown in Figure 2-2. See Table 1-1 for selection of the appropriate socket adapter for the devices you are programming.

2.4 PERIPHERAL CONNECTION

Depending on the data entry mode you use, a CRT terminal, computer, or tape reader may be connected to the programmer. The programmer's serial port connector-pin functions are detailed in Section 2 of the programmer's instruction manual.

Set the CRT's status switches as follows:

- No Parity
- 8-bit Word Width
- Full Duplex
- RS232C Enabled
- 1 Stop Bit
- Upper Case

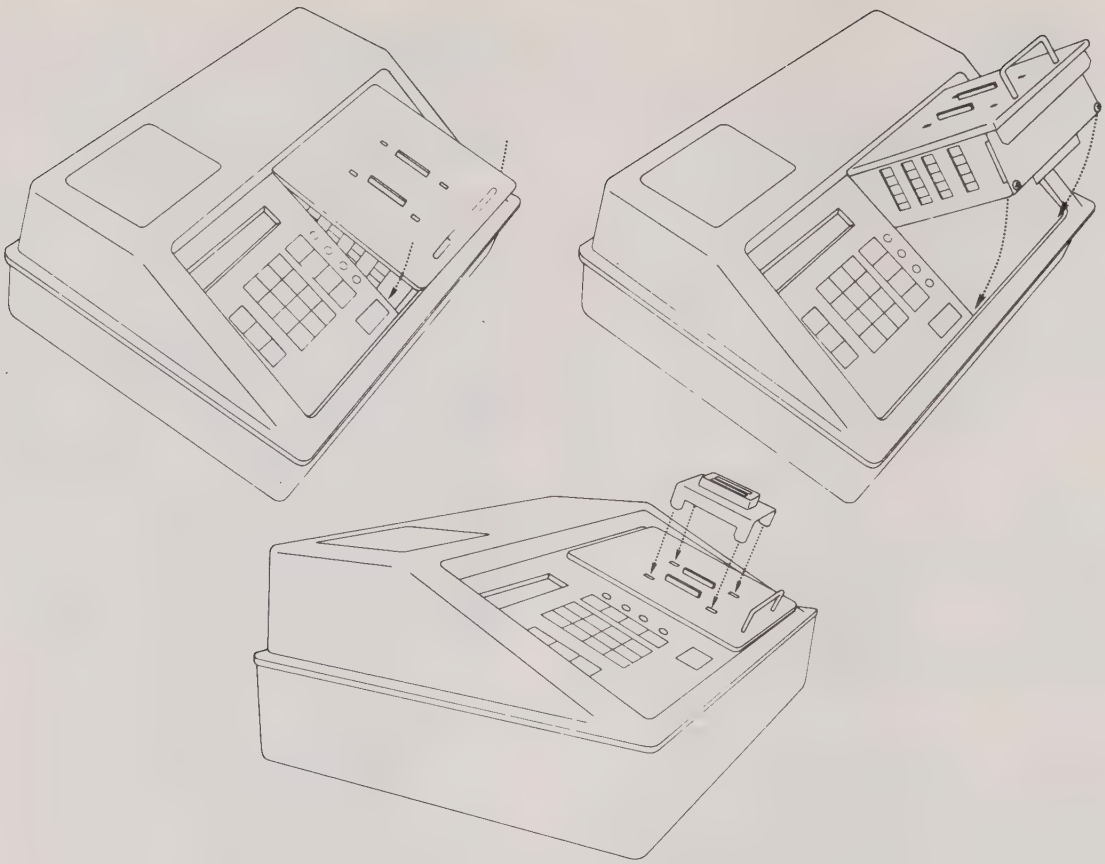


Figure 2-2. Programming Module and Socket Adapter Installation

2.5 FRONT PANEL LABELS

As stated in section 1.2, one way to enter logic states is from the System 19 keyboard. Vinyl labels are provided with the Logic Pak to facilitate keyboard entry on the System 19 front panel. The keypad label tells you what the six hex displays mean while using the front panel logic entry mode.

While entering logic states, ignore the words ADDRESS and DATA on the label. These designations are meaningful only when you are programming memory devices.

Figure 2-3 shows how to attach the labels.

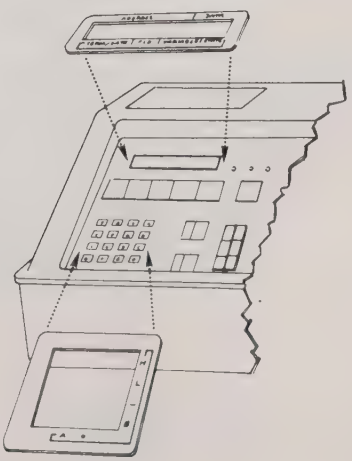


Figure 2-3. Installing the System 19 Keypad and Display Labels

SECTION 3
OPERATION

3.1 INTRODUCTION

Programmable logic devices are arrays of logic elements joined by matrices of fusible links. Appendix A contains logic diagrams of the five Signetics IFL devices programmed by this module. You can custom design a logic circuit by burning selected fuses in the matrices. Figure 3-1 shows the programming options of each fuse matrix and which fuses must be blown to create each logic function.

3.1.1 THE PROCESS

There are three basic steps to follow when you program a logic device:

1. Prepare a function (truth) table just as you would when designing with discrete logic.

2. Transfer the function table into the programmer's data RAM.

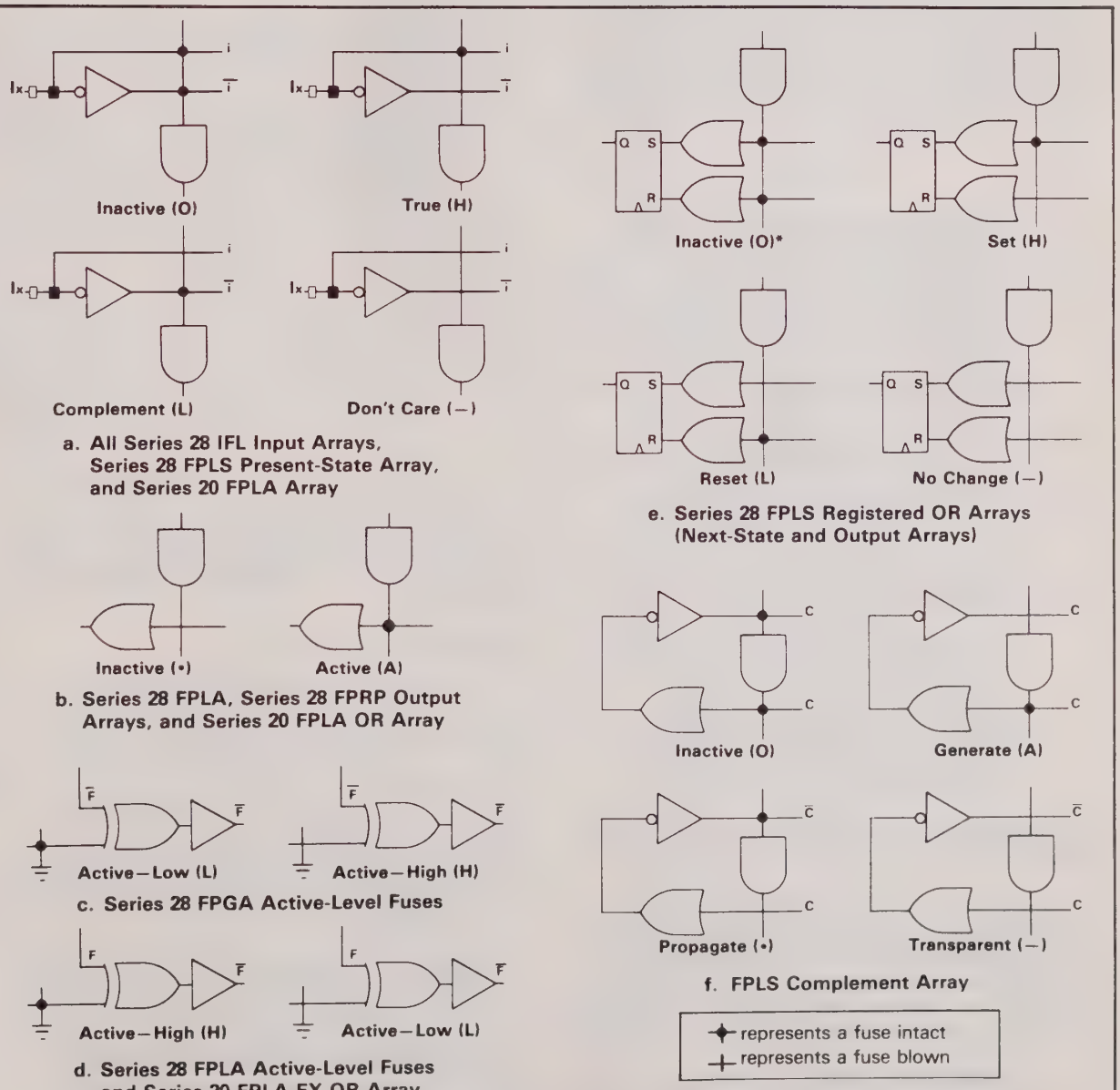

Inactive (O)
True (H)
Complement (L)
Don't Care (—)
a. All Series 28 IFL Input Arrays, Series 28 FPLS Present-State Array, and Series 20 FPLA Array
Inactive (O)*
Set (H)
Reset (L)
No Change (—)
e. Series 28 FPLS Registered OR Arrays (Next-State and Output Arrays)
Inactive (•)
Active (A)
b. Series 28 FPLA, Series 28 FPRP Output Arrays, and Series 20 FPLA OR Array
Inactive (O)
Generate (A)
Propagate (•)
Transparent (—)
f. FPLS Complement Array
Active—Low (L)
Active—High (H)
c. Series 28 FPGA Active-Level Fuses
Active—High (H)
Active—Low (L)
d. Series 28 FPLA Active-Level Fuses and Series 20 FPLA EX-OR Array
represents a fuse intact
represents a fuse blown
* To prevent exciting both S and R flip-flop inputs simultaneously, this state is only allowed for OR gates driven by inactive AND gates.

Figure 3-1. IFL Programming Options

3. Program a blank device.

NOTE

If you already have a programmed master device, you can load the data into the programmer and skip steps 1 and 2 given above. See your programmer manual for procedures.

The first step is common to any logic design process. Your function table cannot exceed the size of the device. The table should be formatted as sets of input variables and corresponding sets of output states, set against each other. Each set of input and output conditions is considered a term or gate for data entry to the programmer.

The second step, transferring the function table into the programmer's data RAM, is covered in detail in this section. The third step, programming a blank device, is covered in the manual for the specific programmer you are using.

CAUTION

The correspondence between locations used in the programmer RAM to program specific fuses in the devices has been changed in this hardware (950-0104) versus the earlier 919-1542 and 950-0800. If you are loading data into the programmer via the port using a PROM-type data format (hexadecimal for example) you must prepare new paper tapes or data files for use with the 950-0104. Failures to do so will result in improperly programmed devices. If you are using master devices as your data source or are loading data via the port using the logic format, this change is transparent to you.

New tapes or files can be prepared by first programming a master device using the earlier hardware and tapes. Next, install the 919-0104 and load the data into RAM. Then download the data out the port to your tape punch or other storage medium.

3.1.2 PRELIMINARY INFORMATION ON USING THE PROCEDURES IN THIS MANUAL

The Logic Pak will work in the Data I/O System 17, System 19, Model 100A Production Programmer, or the 29A Universal Programmer. Figure 3-2 is a flowchart showing the overall procedure and options for programming logic devices. Read the information in this section thoroughly before entering data or programming devices.

3.2 PROGRAMMING ALGORITHMS

The Logic Pak uses Signetics' suggested programming algorithm for each array of each device. Refer to the Timing

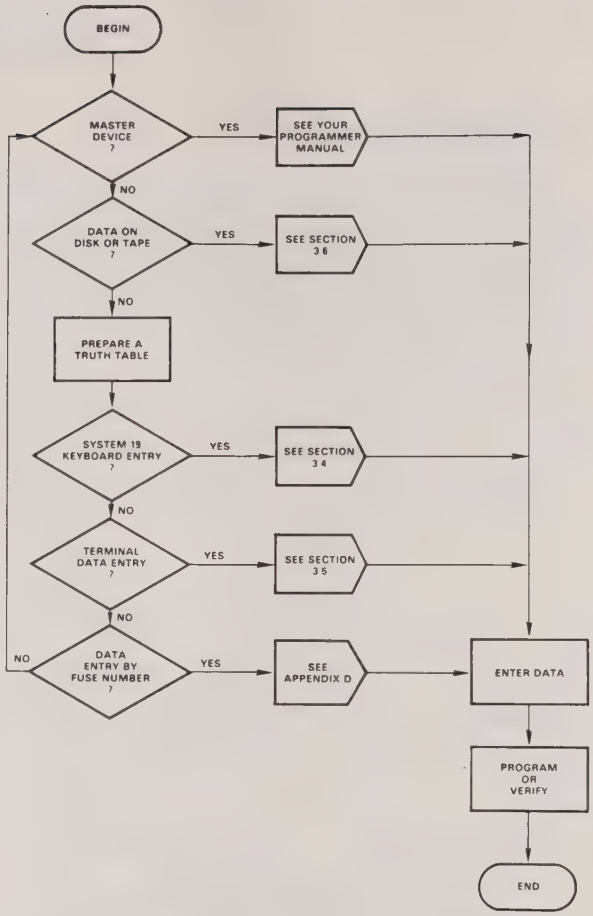


Figure 3-2. Flowchart, Programming Logic Devices

Diagrams in Section 4 for the exact voltages levels and pulse widths.

3.2.1 SERIES 28 FPGA

The output active-level fuses are read before programming the Series 28 FPGA. This is because the input fuses are read through the output active level gates.

Output Active Level. All inputs are raised to the V_{IHH} level, V_{CC} is set to its program level, and the output to be programmed is set to the V_{OP} level. Chip Select is then pulsed to V_{IHH} to control the duration of the programming pulse. Read voltages are presented, and the programmed output is verified against RAM.

Input Gates. All inputs except the one to be programmed are raised to V_{IHH}. The input to be programmed is left at TTL Ø if the true state is to be programmed, or at TTL 1 if the false state is to be programmed. V_{CC} is set to its program level. The outputs of the gates not being programmed are left at the TTL 1 level, while the output of the gate to be programmed is set to V_{OP}. To control the programming-pulse duration, Chip Select is pulsed to TTL Ø. The output used for programming is then verified.

3.2.2 SERIES 28 FPLA

For each product term, the input array fuses are programmed before the output array fuses. The output active level fuses must be read before output array programming because the output array is read through the output active-level gates.

Output Active Level. All inputs are set to V_{IHH} (TTL 1). V_{CC} is grounded, and Chip Select is set to V_{IHH}. A programming pulse is applied to the output to be programmed while all other outputs are left at TTL 1. The Program pin stays at V_V. The programmed output is then verified.

Input AND Array. The product term address is presented to six of the Series 28 FPLA output lines. All inputs except the one to be programmed are raised to V_{IHH}. The input to be programmed is left at TTL Ø if the true fuse is to be blown or at TTL 1 if the false fuse is to be blown, and a programming pulse is applied to the Program pin. To control the duration of the programming pulse, the programmer pulses Chip Enable to TTL 1. The programmed input is then verified via output F_7.

Output OR Array. The product term address is presented to five of the Series 28 FPLA inputs, and V_{CC} is raised to V_P. The output to be programmed is raised to V_{OP}, and all others are left at TTL 1. A programming pulse is applied to the Program pin. To control the programming-pulse duration, Chip Enable is pulsed to V_{IHH}. Finally, the programmed output is verified.

3.2.3 SERIES 28 FPRP

To program a Series 28 FPRP, the Logic Pak uses the routine described for the Series 28 FPLA, but there are no output active-level fuses to program.

NOTE

Attempting to program a Series 28 FPRP with output active-level data does not damage the device, but the programmer displays a programming error code.

3.2.4 SERIES 28 FPLS

Two test terms, transition terms 48 and 49, are automatically programmed before the main arrays are addressed. These are used by Signetics for diagnostic pusposes and cannot be programmed by the customer.

PR/$\overline{OE}$ Option. Device pin 19 is a preset line in virgin devices. The option fuse is blown to change it to the output enable function. The input levels for programming the option fuses are don't cares. V_{CC} is set to V_{CCP}, and the PR/$\overline{OE}$ pin is pulsed to V_{IHH}. Programming is verified via $F_Ø$.

AND Array. The column and row addresses are presented to the FPLS inputs as TTL levels. Input I_{13} is set to TTL 1 to select the AND array, and input I_{14} is set to TTL 1 to select the Program mode. V_{CC} is set to V_{CCP}, CLK is set to V_{PP}, and I_{15} is pulsed to TTL Ø to control the programming-pulse duration. All outputs are left at the TTL 1 level. The fuses are verified one at a time via output FØ.

OR Array. The procedure for programming the OR array is the same as for the AND array in all respects except Input I_{13} is set to TTL Ø to select the OR array.

3.2.5 SERIES 20 FPLA

The AND, OR, and active level arrays are programmed identically. With V_{CC} at GND and B_8 at V_{FVV}, select the fuse to be programmed by applying the column and new address to the input as TTL levels. Set B_1 to V_{IHH} and B_7 to V_{IL}. After T_D delay raise V_{CC} to V_{CCP}. After T_D delay raise B_7 to V_{IHH}. After another T_D delay, raise B_8 to V_{PP}. Following T_D delay, pulse B_1 to V_{IL} for a duration for T_P. Wait T_D and return B_8 to V_V and then T_D after that return B_7 to V_{IL}.

3.2.6 REJECT JUMPER

The Logic Pak makes a limited number of attempts to burn each fuse. If the fuse does not verify after the specified number of attempts, the programmer will halt and signal an error. The maximum number of pulses is set by JP1 on Analog Card #1 (shown in Figure 4-2). JP1 should be left in position A (one pulse attempt before reject).

3.3 PREOPERATIONAL PROCEDURES

Before you attempt to enter logic states, complete the steps outlined in the following paragraphs:

1. Install the Logic Pak and appropriate socket adapter in the programmer.

2. Be sure the programmer is properly connected to any other equipment you are using. This is described in Section 2 of this manual.

   NOTE

   Though the 29A Universal Programmer normally communicates with peripherals in half duplex, full duplex is required when using it with the 950-0104 Logic Pak.

3. Turn on the programmer and any other equipment in the system.

4. Enter the data entry mode you wish to use. These are listed in Table 3-1. The procedures are given in the following paragraphs.

3.3.1 ENTERING THE FRONT PANEL DATA ENTRY MODE (EØ)

Data can be entered via the front panel only when using a System 19 programmer. The procedure is as follows:

1. Press SEL

Table 3-1. Data Entry Modes

CODE	DESCRIPTION	NOTES
EØ	Front Panel Data Entry	*1, 2*
E1	Terminal Data Entry	*2*
E2	Serial Input	
E3	Serial Output	
EE	Data Entry by Fuse Number	*3*

1. With System 19s only.
2. Will not work with programmers using Computer Remote Control.
3. Refer to Appendix D for procedures.

2. Enter EØ.

3. Press START. The display will look like Figure 3-3.

3.3.2 ENTERING THE TERMINAL DATA ENTRY MODE (E1)

E1 is used when you are using a System 17, 19 or a 29A Universal Programmer. The key sequences for entering this mode are:

1. Press SELECT
2. Enter E1
3. Press START

The display will look like one of the title blocks in Figure 3-4.

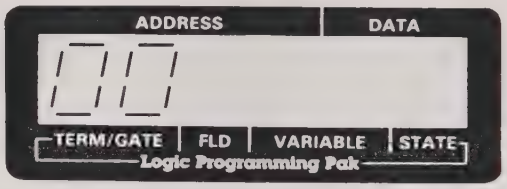
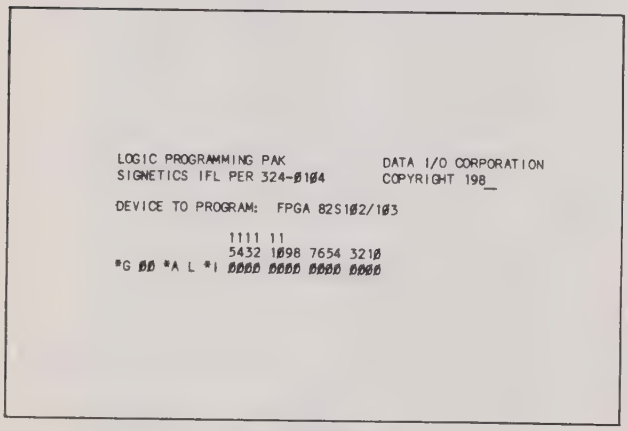
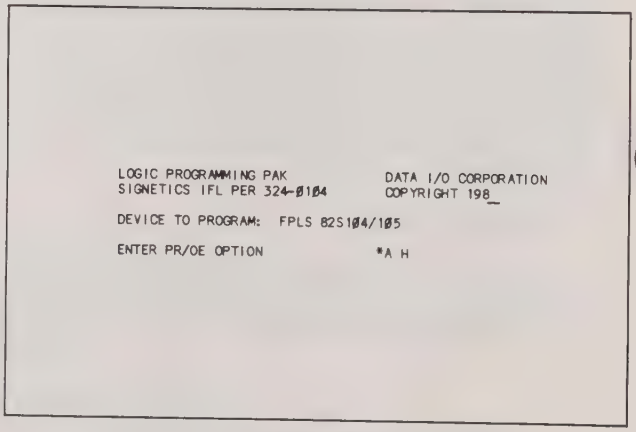


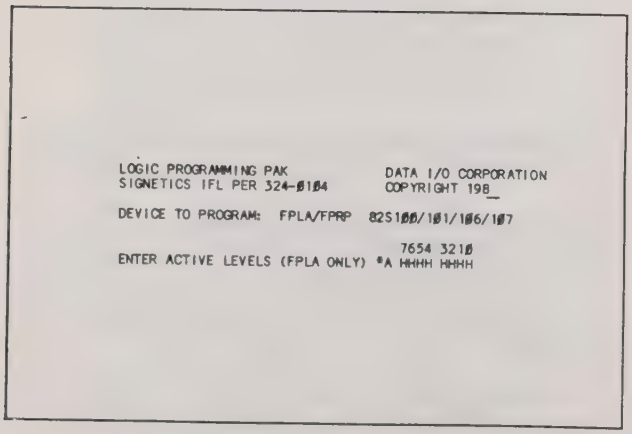
Figure 3-3. System 19 Display After Entering the Front Panel Data Entry Mode (EØ)


LOGIC PROGRAMMING PAK
SIGNETICS IFL PER 324-ØlØ4
DATA I/O CORPORATION
COPYRIGHT 198_
DEVICE TO PROGRAM: FPGA 82S1Ø2/1Ø3
1111 11
5432 1Ø98 7654 321Ø
*G ØØ *A L *I ØØØØ ØØØØ ØØØØ ØØØØ

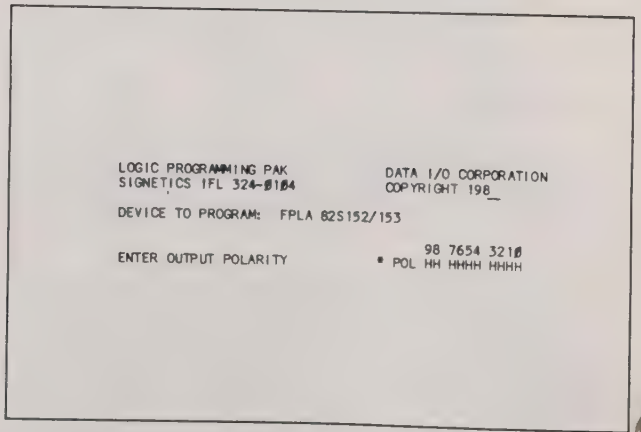
a. Series 28 FPGA



c. Series 28 FPLS



b. Series 28 FPLA/FPRP



d. Series 20 FPLA

Figure 3-4. CRT Display After Entering the Terminal Data Entry Mode.

* The v character is used to denote the space bar.

3.3.3 ENTERING THE SERIAL INPUT OR SERIAL OUTPUT MODES (E2 AND E3)

Serial input and output can be done from the System 17 or 19, 29A Universal Programmer, or 100A Production Programmer. Select Functions E2 and E3 can be entered from the System 19 keyboard or through remote control on the 17, 19, 29A or 100A. Key sequences on the programmer are the same as those used for entering other Select Functions or Select Codes.

3.4 FRONT PANEL DATA ENTRY

When using the System 19 front panel data entry mode, you are presented with a series of "fields" which correspond to the device arrays. Each field contains a series of variables. You key in a logic state for each variable, one at a time. The following paragraphs explain the procedures.

3.4.1 THE DISPLAY

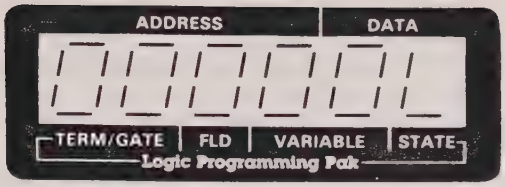
Enter a gate or term number and press ENTER. If no number is entered, the default value Ø0 will appear. Next, enter a field number and press ENTER. If no number is entered, the default value Ø will appear.

Refer to Figure 3-5. Enter a variable number and press ENTER. If no number is entered, the highest numbered variable in the field for that device will appear.

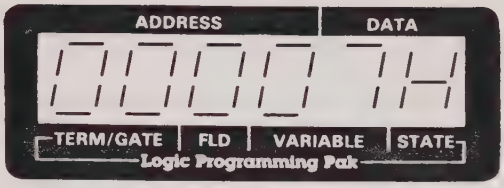
NOTE

The display is determined by the socket adapter installed in the Logic Pak.

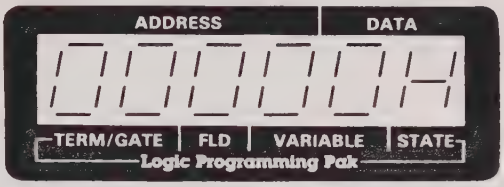
Left to right, the first two characters represent the decimal number of the gate or term you are working on. The next character is the number of the field whose variables are being set. Table 3-2 lists the field numbers of the various arrays. The next two characters are the decimal number of the variable which will receive the next logic entry. The highest-numbered variable will appear first. The right-most character shows the current state of the variable.



a. Series 28 FPGA



b. Series 28 FPLA/FPRP



c. Series 28 FPLS

D. Series 20 FPLA

Figure 3-5. System 19 Display After Entering EØ and Pressing ENTER 3 Times.

Table 3-2. Field Numbering for Front Panel Entry

FIELD NUMBER	SERIES 28 FPGA	SERIES 28 FPLA/FPRP	SERIES 28 FPLS	SERIES 20 FPLA
Ø	Active Level	Active Levels	PR/$\overline{OE}$ Option	Output Polarities
1	Input Array	Input Array	Complement Array	Input Array
2	NA	Output Array	Input Array	B(I) Input Array
3	NA	NA	Present State Array	B(O) Output Array
4	NA	NA	Next State	NA
5	NA	NA	Output Array	NA

3.4.2 THE KEYPAD

Figure 3-6 shows the System 19 keyboard configured for use with the Logic Pak. The six keys named by the keypad overlay are the logic states. The instructions for each device (paragraph 3.4.3) explain the logic states represented by the characters on the overlay. Pressing any logic state key both enters that state to the displayed variable and steps the display to the next variable. The ENTER and REVIEW keys can be used to step through the variables without entering any logic states. (ENTER steps you forward and REVIEW backwards.)

The first variable in each field is always the highest numbered variable, allowing you to enter states as they appear, left to right, on the data entry tables available from Signetics.

When you step past the lowest variable in a field, the display rolls over to the highest variable of the next higher field. Likewise, stepping down past the highest variable causes a rollover to the lowest variable of the next lower field.

When the field counter rolls over, the term/gate counter increments or decrements. The term/gate counter can also be incremented with the EDIT key. A new gate or term number can be entered directly by pressing SELECT and entering the new number.

3.4.3 LOGIC ENTRY

The following paragraphs explain keyboard logic entry for each device programmed by the Logic Pak.

SERIES 28 FPGA. The display shown in Figure 3-5a indicates you are looking at Field Ø, the Output Active Level Array of Gate Ø. Variable ØØ is Output FØ and currently is at the default value L (Low). Table 3-3 lists the meaning of the valid logic entries for all fields in the Series 28 FPGA.

Press This Key	To Enter This State
A	H
B	L
C	-
D	Ø
E	•
F	A

Figure 3-6. System 19 Keyboard.

Table 3-3. Series 28 FPGA Logic Entry

CHARACTER	OUTPUT ACTIVE LEVEL	INPUT ARRAY
H	HIGH	TRUE
L	LOW	FALSE
-	NA	DON'T CARE
Ø	NA	INACTIVE

1. Enter the Output Active level from your function table. The field counter will advance. You are now in the Input Array of Gate Ø.

2. Enter the Input states for the gate. When you finish, the gate counter will step to Gate 1.

3. Enter logic states for the product term's Output Array. When you finish, the term/gate counter will increment and the field counter will return to 1, the Input Array field.

4. Repeat steps 1 and 2 until you have entered all of the states from your function table.

5. Step through the variables again, starting with Gate Ø. Check each entry against your function table.

6. Press KEYBD.

7. Insert a device in the socket adapter and start a Program operation.

SERIES 28 FPLA/FPRP. The display shown in Figure 3-5b indicates Field Ø, the Output Active Level Array. The term/gate counter is irrelevant to this field. Variable Ø7 is Output F_7 and is currently at the default state, H (High). Table 3-4 lists and describes the functions of the various state entries used in the different fields of the Series 28 FPLA and FPRP.

Table 3-4. Series 28 FPLA/FPRP Logic Entries

ENTER	SERIES 28 FPLA ACTIVE LEVEL	INPUT ARRAY	OUTPUT ARRAY
H	HIGH	TRUE	NA
L	LOW	FALSE	NA
–	NA	DON'T CARE	NA
Ø	NA	INACTIVE	NA
A	NA	NA	ACTIVE
•	NA	NA	INACTIVE

1. *Series 28 FPLA:* Enter the active levels for the Series 28 FPLA outputs. When you enter the last one, the field counter will increment. You are now in the Input Array of Product Term ØØ and ready to enter a state for I_{15}, whose default value appears in the far right display.

Series 28 FPRP: Press ENTER repeatedly until the Field counter steps to 1. Do not enter states for Field Ø or a programming error will occur in step 7.

2. Enter logic states for the product term inputs. When you finish, the field counter will step to 2, the Output Array field.

3. Enter logic states for the product term's Output Array. When you finish, the term/gate counter will increment and the field counter will return to 1, the Input Array field.

4. Repeat steps 2 and 3 until you've entered all of the states from your function table.

5. Step through the variables again, starting with the Active Level field. Check each entry against you function table.

6. Press KEYBD

7. Insert a blank device in the socket adapter and start a Program operation.

SERIES 28 FPLS. Figure 3-5c indicates Field Ø, the Preset/Output Enable (PR/$\overline{OE}$) option. The term/gate counter is irrelevant to this field. The single variable ØØ in this field is currently at the default value, H (Preset). Table 3-5 lists and describes the functions of the various state entries used in the different fields of the FPLS.

1. Enter the PR/$\overline{OE}$ option. The field counter will increment and you will then be in field 1, the Complement Array of Transition Term ØØ.

2. Enter a state for the single variable of the Complement Array. The field counter will step to the Input Array field.

3. Enter states for the Input Array. When you complete the field, the field counter will step to the Present State Array field.

4. Enter states for the Next State Array field. As you finish this field, the field counter will step to the Output Array field.

5. Enter states for the Output Array. When you finish, the field counter will return to 1, the Complement Array, and the term counter will step to the next transition term.

6. Repeat steps 2 through 5 until you've entered all of the states from your function table.

7. Review all of your entries, beginning with field Ø. Check each entry against your function table.

8. Press KEYBD.

9. Insert a blank device in the socket adapter and start a Program operation.

SERIES 20 FPLA. The initial display (Figure 3-5d) indicates Field Ø, the output polarity field. The term/gate counter is irrelevant to this field, Variable Ø9 is output F9 and is currently at the default state, H (High). Table 3-6 lists and describes the functions of the various state entries used in the different fields of this FPLA.

1. Enter the output polarities for the FPLA outputs. When you enter the last one, the field counter will increment. You are now in the Input Array of product term ØØ and ready to enter a state for 17, whose default value appears in the far right display.

2. Enter logic states for the product term inputs. When you finish, the field counter will step to 2, the B(I) Input Array.

3. Enter logic states for the product term's B(I) Input Array. When you finish, the field counter will step to 3, the B(O) Output Array. Note that this field does not exist for product terms 32 through 41.

4. Enter logic states for the product term's B(O) Output Array. When you finish, the term/gate counter will

Table 3-5. Series 28 FPLS Logic Entry

CHARACTER	PR/$\overline{OE}$	COMPLEMENT ARRAY	INPUT & PRESENT STATE ARRAYS	NEXT STATES & OUTPUT ARRAYS
H	PRESET	NA	TRUE	SET
L	OUTPUT ENABLE	NA	FALSE	RESET
-	NA	TRANSPARENT	DON'T CARE	NO CHANGE
Ø	NA	INACTIVE	INACTIVE	INACTIVE
A	NA	GENERATE	NA	NA
•	NA	PROPAGATE	NA	NA

Table 3-6. Series 20 FPLA Logic Entry

CHARACTER	ACTIVE LEVEL	I ARRAY	B(I) ARRAY	B(O) ARRAY
H	HIGH	TRUE	TRUE	NA
L	LOW	FALSE	FALSE	NA
-	NA	DON'T CARE	DON'T CARE	NA
Ø	NA	INACTIVE	INACTIVE	NA
A	NA	NA	NA	ACTIVE
●	NA	NA	NA	INACTIVE

counter and the field counter will return to 1, the Input Array field.

5. Repeat step 2 through 4 until you have entered all the states from your function table.

6. Step through the variables again, starting from the output polarity fields. Check each entry against your function table.

7. Press KEYBD.

8. Insert a blank device in the socket adapter and start a Program operation.

NOTE

Control terms are numbered as follows:

Control Term No.	*Term/Gate No.*
D9	*32*
D8	*33*
D7	*34*
D6	*35*
D5	*36*
D4	*37*
D3	*38*
D2	*39*
D1	*40*
D0	*41*

3.5 TERMINAL DATA ENTRY

When using the terminal entry mode, you are presented with a series of "fields" corresponding to the various arrays within a device you will later program. To load RAM with your function table, key in logic state characters to the variables in these fields. The title block you see on the screen includes the first field for the device you are working with.

The following paragraphs explain how to put logic states (data) in at the proper locations and how to use the terminal to edit data after it has been entered.

3.5.1 COMMANDS

Table 3-7 lists the editing commands you can use to manipulate logic entries, control the display, and move the cursor.

3.5.2 LOGIC ENTRY

The following paragraphs explain terminal logic entry for each device programmed by the Logic Pak.

SERIES 28 FPGA. The CRT screen will look like Figure 3-4a. Table 3-3 lists the valid logic state entries for the Series 28 FPGA.

1. Enter a gate number. The cursor will then move to the single variable for the Output Active Level field.

2. Enter a state for the Output Active Level. The cursor will then move to the first variable of the Input Array field.

3. Enter states for the Input Array variables.

4. When you finish a gate's variables, the next gate's variables will appear and the cursor will return to the Active Level variable. Repeat steps 2 and 3 for each gate, until you have loaded all of the function table.

5. When you are finished, check the gates against your function table, and be sure you've entered the proper logic state for each variable.

6. Press ESCAPE.

7. Insert a blank device in the socket adapter and start a Program operation.

SERIES 28 FPLA/FPRP. The CRT screen will look like Figure 3-4b. Table 3-4 lists the logic entries to use for these devices.

1. *Series 28 FPLA only:* Enter the Active Levels for the product term outputs.

Table 3-7. Terminal Editing Commands

COMMAND NAME		DESCRIPTION
G	Enter Gate Number	Cursor waits for entry of an FPGA gate number.
P	Enter Product Term Number	Cursor waits for an entry of an FPLA/FPRP product term number.
T	Enter Transition Term Number	Cursor waits for entry of an FPLS transition term number.
>	Advance Cursor	Moves cursor to the right.
<	Back up Cursor	Moves cursor to the left.
F	Display Next Term	Display next-highest numbered gate or term.
R	Display Last Term	Display next-lowest numbered gate or term.
N	Enter Next Field	Cursor advances to the next field of variables in the current gate or term.
I	Insert Term	The displayed term will show its default (virgin) values; new states can then be entered. Higher-numbered terms move up one term. Highest device term is lost. See Figure 3-7. (Takes several seconds to execute.)
D	Delete Term	Data at displayed term is destroyed. Data at higher-numbered terms moves down one term. See Figure 3-8.
C	Clear Term	Displayed term is cleared to its default values.
X	Deactivate Term	Outputs of displayed term are set to inactive. FPLA and FPLS only.
E	Enter Edit Mode	On entering the Edit Mode, a menu appears listing the Edit mode.
1	List Low-Order Terms	Terms 0-23 are displayed.
2	List High-Order Terms	Terms 24-27 are displayed.
3	Compress Terms	Non-consecutive terms are moved up to occupy intervening blank terms. See Figure 3-9.
4	Verify Device	The screen will display nonverifying data: RAM data will appear first, with corresponding device data on the line below. This function is described more fully in paragraph 3.7.1.
S	Enter Select Mode	On entering the Select Mode, a menu appears, listing the commands for the entering three of the Logic Pak operating modes.
1	Terminal Entry	
2	Serial Input	
3	Serial Output	
ESCAPE	Escape Logic Entry	Press ESCAPE on the terminal returns control to the instrument from which the logic-entry mode was entered: the programmer keyboard or Remote Control.
CTL S	Halt Transmission	Use this command to interrupt Serial Output or Verify Output
CTL Q	Resume Transmission	Use this command to resume transmission after interrupting Serial Output or Verify Output

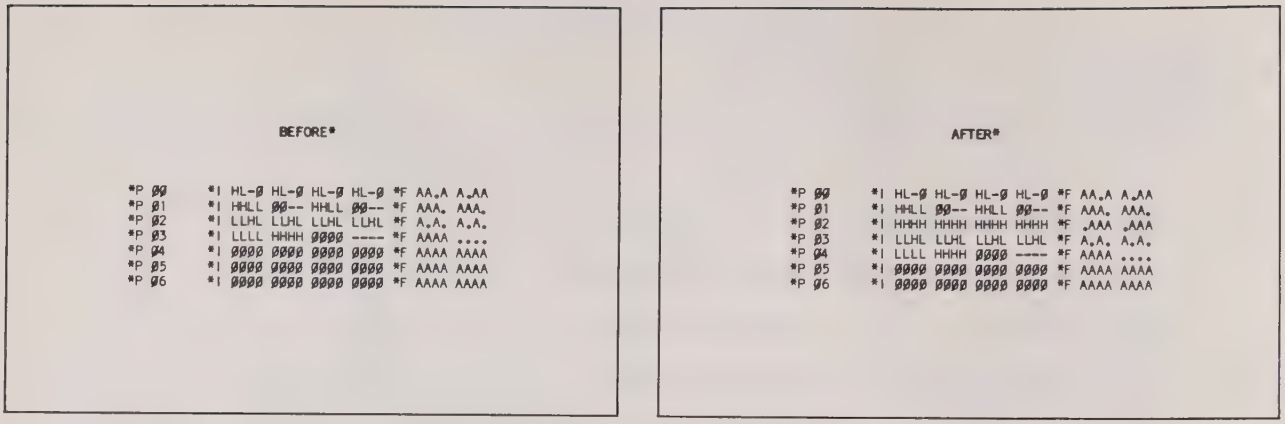

BEFORE*
*P ØØ *I HL-Ø HL-Ø HL-Ø HL-Ø *F AA.A A.AA
*P Ø1 *I HHLL ØØ-- HHLL ØØ-- *F AAA. AAA.
*P Ø2 *I LLHL LLHL LLHL LLHL *F A.A. A.A.
*P Ø3 *I LLLL HHHH ØØØØ ---- *F AAAA ....
*P Ø4 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø5 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø6 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
AFTER*
*P ØØ *I HL-Ø HL-Ø HL-Ø HL-Ø *F AA.A A.AA
*P Ø1 *I HHLL ØØ-- HHLL ØØ-- *F AAA. AAA.
*P Ø2 *I HHHH HHHH HHHH HHHH *F .AAA .AAA
*P Ø3 *I LLHL LLHL LLHL LLHL *F A.A. A.A.
*P Ø4 *I LLLL HHHH ØØØØ ---- *F AAAA ....
*P Ø5 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø6 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA

Figure 3-7. Insert Series 28 FPLA Data

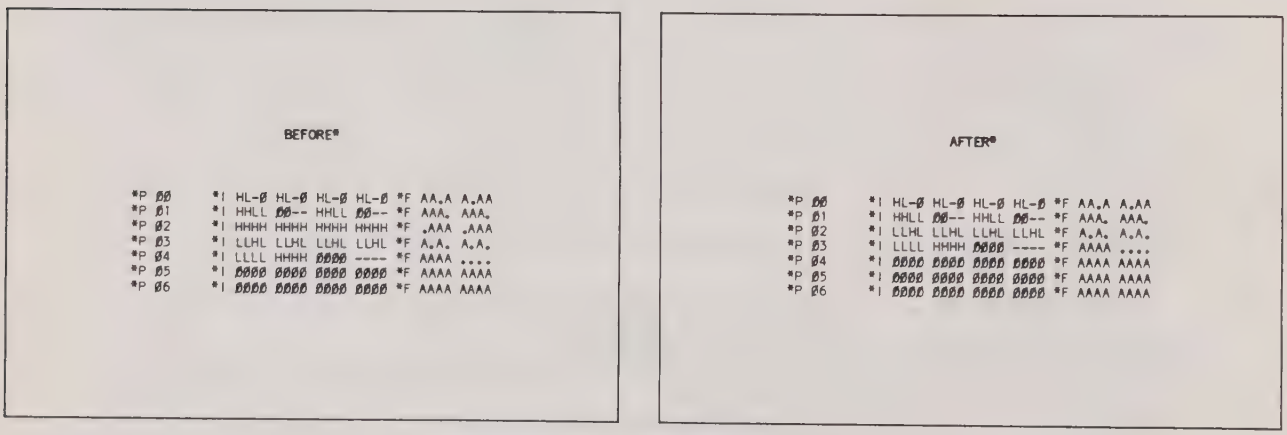

BEFORE*
*P ØØ *I HL-Ø HL-Ø HL-Ø HL-Ø *F AA.A A.AA
*P Ø1 *I HHLL ØØ-- HHLL ØØ-- *F AAA. AAA.
*P Ø2 *I HHHH HHHH HHHH HHHH *F .AAA .AAA
*P Ø3 *I LLHL LLHL LLHL LLHL *F A.A. A.A.
*P Ø4 *I LLLL HHHH ØØØØ ---- *F AAAA ....
*P Ø5 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø6 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
AFTER*
*P ØØ *I HL-Ø HL-Ø HL-Ø HL-Ø *F AA.A A.AA
*P Ø1 *I HHLL ØØ-- HHLL ØØ-- *F AAA. AAA.
*P Ø2 *I LLHL LLHL LLHL LLHL *F A.A. A.A.
*P Ø3 *I LLLL HHHH ØØØØ ---- *F AAAA ....
*P Ø4 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø5 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø6 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA

Figure 3-8. Delete Series 28 FPLA Data

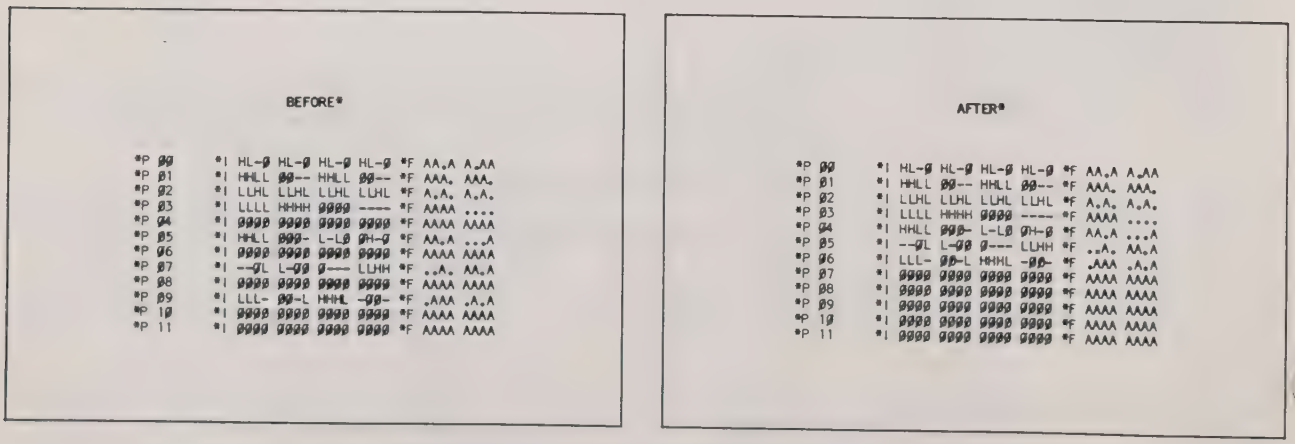

BEFORE*
*P ØØ *I HL-Ø HL-Ø HL-Ø HL-Ø *F AA.A A.AA
*P Ø1 *I HHLL ØØ-- HHLL ØØ-- *F AAA. AAA.
*P Ø2 *I LLHL LLHL LLHL LLHL *F A.A. A.A.
*P Ø3 *I LLLL HHHH ØØØØ ---- *F AAAA ....
*P Ø4 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø5 *I HHLL ØØØ- L-LØ ØH-Ø *F AA.A ...A
*P Ø6 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø7 *I --ØL L-ØØ Ø--- LLHH *F ..A. AA.A
*P Ø8 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø9 *I LLL- ØØ-L HHHL -ØØ- *F .AAA .A.A
*P 1Ø *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P 11 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
AFTER*
*P ØØ *I HL-Ø HL-Ø HL-Ø HL-Ø *F AA.A A.AA
*P Ø1 *I HHLL ØØ-- HHLL ØØ-- *F AAA. AAA.
*P Ø2 *I LLHL LLHL LLHL LLHL *F A.A. A.A.
*P Ø3 *I LLLL HHHH ØØØØ ---- *F AAAA ....
*P Ø4 *I HHLL ØØØ- L-LØ ØH-Ø *F AA.A ...A
*P Ø5 *I --ØL L-ØØ Ø--- LLHH *F ..A. AA.A
*P Ø6 *I LLL- ØØ-L HHHL -ØØ- *F .AAA .A.A
*P Ø7 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø8 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P Ø9 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P 1Ø *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA
*P 11 *I ØØØØ ØØØØ ØØØØ ØØØØ *F AAAA AAAA

Figure 3-9. Compress Series 28 FPLA Terms

2. Press P. You'll see the two product term fields displayed, as in Figure 3-10.

3. Enter the number of the product term you want to work on. The cursor will then be under the first variable of the Input Array field.

4. Enter logic states for the Input Array variables.

5. After setting the last variable in the field, the cursor will jump to the next field, the Output Array variables.

6. When you finish the term, the cursor will return to the first variable of the Input Array field, and the product term number will increment. Repeat steps 4 and 5 until you've entered all of your function table.

7. Check all of the product terms against your function table.

8. Press ESCAPE.

9. Insert a blank device in the socket adapter and start a Program operation.

SERIES 28 FPLS. The CRT screen will look like Figure 3-4c. Table 3-5 lists the valid logic states for the Series 28 FPLS.

1. Enter the PR/$\overline{OE}$ option variable.

2. Press T. The five fields of the transition terms will appear on the screen as in Figure 3-11.

3. Enter the number of the transition term you want to work on. The cursor will then be under the variable in the Complement Array field.

4. Enter a state for the Complement Array. The cursor will then move to the first variable of the next field.

5. Enter states for the variables in the Input Array field. The cursor will then move to the first variable in the next field.

6. Enter characters for the Present State Array field. The cursor will then jump to the first variable of the next field.

7. Enter logic states for the Next State Array field. The cursor will then move to the first variable in the last field.

8. Enter logic states for the Output Array field. When you finish, the cursor will return to the variable in

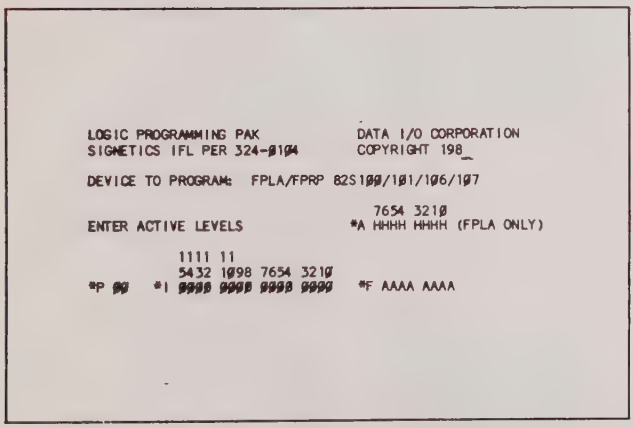


Figure 3-10. Series 28 FPLA/FPRP Title Block and Product Term ØØ After Pressing P

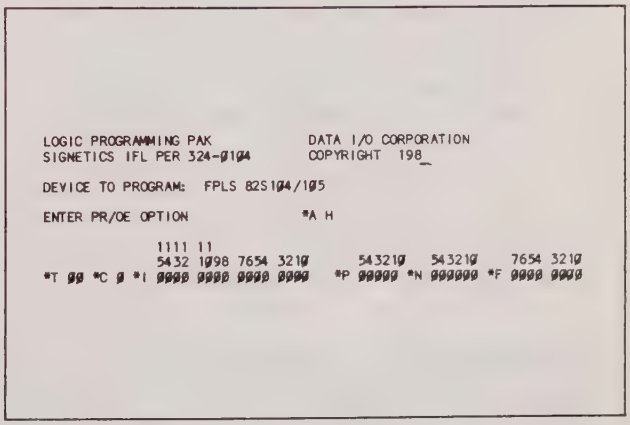

LOGIC PROGRAMMING PAK
DATA I/O CORPORATION
SIGNETICS IFL PER 324-Ø1Ø4
COPYRIGHT 198_
DEVICE TO PROGRAM: FPLS 82S1Ø4/1Ø5
ENTER PR/OE OPTION
*A H
1111 11
5432 1Ø98 7654 321Ø
543210 543210 7654 321Ø
*T ØØ *C Ø *I ØØØØ ØØØØ ØØØØ ØØØØ *P ØØØØØ *N ØØØØØØ *F ØØØØ ØØØØ

Figure 3-11. SERIES 28 FPLS Title Block and Transition Term ØØ After Pressing T

the Complement Array field, and the transition term number will increment.

9. Repeats steps 4 through 8 until you've entered your entire function table.

10. Press ESCAPE.

11. Insert a blank device in the socket adapter and start a Program operation.

SERIES 20 FPLA. The CRT screen will look like Figure 3-4d. Table 3-6 lists the logic entries to use for the Series 20 FPLA.

1. Enter the Active Levels for the product term outputs.

2. Press P. You will see the three product term fields displayed, as in Figure 3-12a.

3. Enter the number of the product term you want to work on. The cursor will then be under the first variable of the Input (I) Array field.

4. Enter the logic states for the I Array variables.

5. After setting the last variable of the field, the cursor will jump to the next field, the B(I) Array variables.

6. Enter the logic states for the B(I) Array variables.

7. Complete the term by entering the logic states of the last field, the B(O) Array variables. Upon completion, the cursor will return to the first variable of the I Array field, and the product term will increment.

8. Repeat steps 4 through 7 until you have entered all of the product terms (P_{00} through P_{31}).

9. Upon completion of the last product term (P_{31}), the cursor will return to the first variable in the I Array field of the first control term (PD_9) as shown in Figure 3-12b.

10. Repeat steps 4 through 6 until you have entered in all of your control terms (PD_9 through PD_0).

11. Check all of the terms against your function table.

12. Press ESCAPE.

13. Insert a blank device in the socket adapter and start a Program operation.

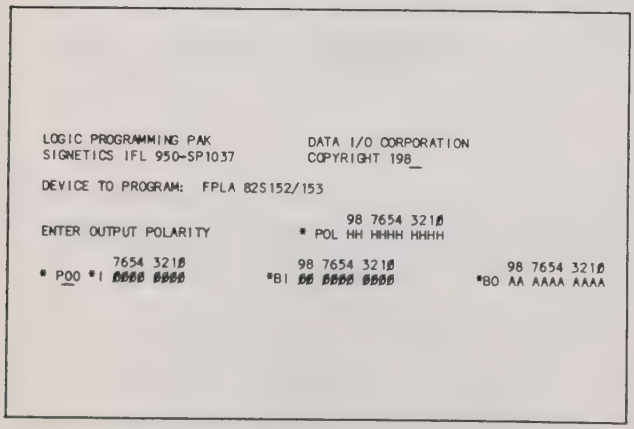
3.6 LOGIC FORMATS FOR SERIAL I/O

When transmitting logic programming data to or from the programmer's serial port, use the ASCII-Logic format described in the following paragraphs.

3.6.1 INPUT (E2)

Figure 3-13 illustrates input files for all five logic devices. Start the stream with an SOH (CTL A) or STX (CTL B), Header information can be included but it must appear before the SOH or STX. Signal the end of transmission with an ETX (CTL C).

Logic states for each array are grouped in fields of variables. Each field is preceded by its own ID code: an



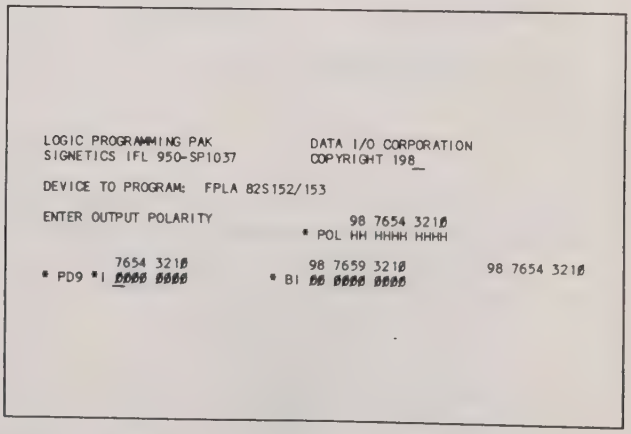
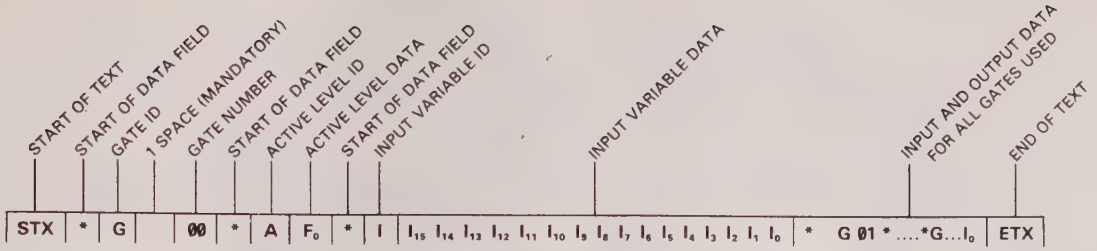
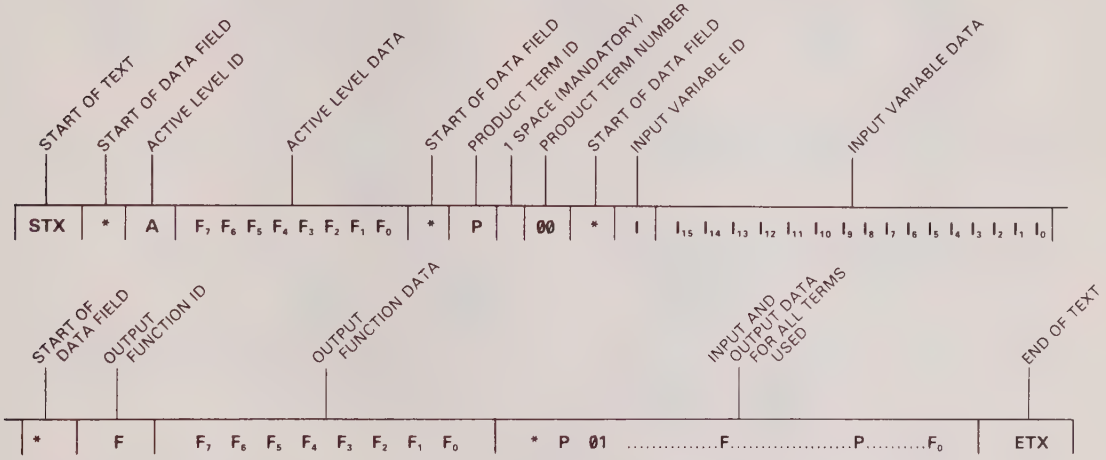


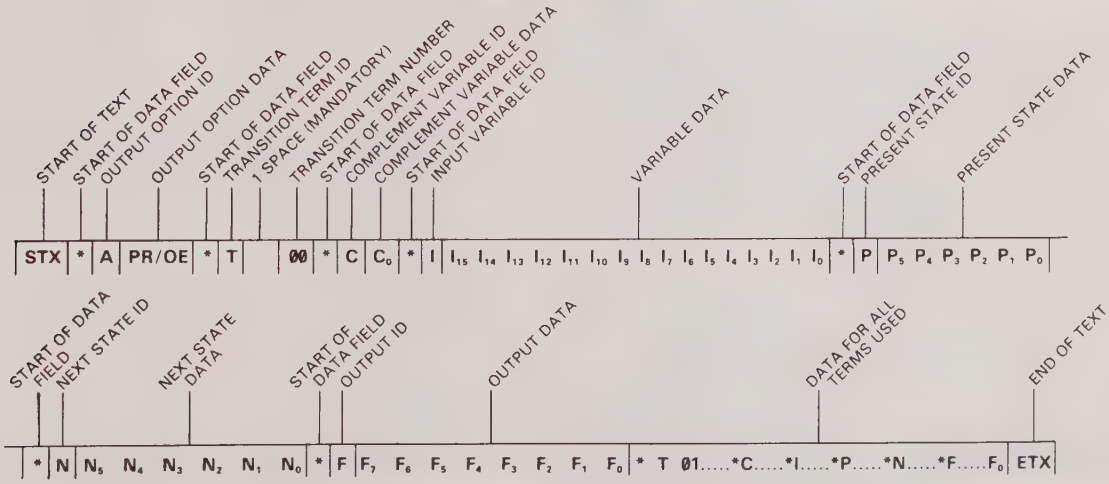
Figure 3-12. Series 20 FPLA Fields.


START OF TEXT
START OF DATA FIELD
GATE ID
1 SPACE (MANDATORY)
GATE NUMBER
START OF DATA FIELD
ACTIVE LEVEL ID
ACTIVE LEVEL DATA
START OF DATA FIELD
INPUT VARIABLE ID
INPUT VARIABLE DATA
INPUT AND OUTPUT DATA FOR ALL GATES USED
END OF TEXT
STX * G 00 * A F0 * I I15 I14 I13 I12 I11 I10 I9 I8 I7 I6 I5 I4 I3 I2 I1 I0 * G 01 * ....*G...I0 ETX

a. Series 28 FPGA


START OF TEXT
START OF DATA FIELD
ACTIVE LEVEL ID
ACTIVE LEVEL DATA
START OF DATA FIELD
PRODUCT TERM ID
1 SPACE (MANDATORY)
PRODUCT TERM NUMBER
START OF DATA FIELD
INPUT VARIABLE ID
INPUT VARIABLE DATA
STX * A F7 F6 F5 F4 F3 F2 F1 F0 * P 00 * I I15 I14 I13 I12 I11 I10 I9 I8 I7 I6 I5 I4 I3 I2 I1 I0
START OF DATA FIELD
OUTPUT FUNCTION ID
OUTPUT FUNCTION DATA
INPUT AND OUTPUT DATA FOR ALL TERMS USED
END OF TEXT
* F F7 F6 F5 F4 F3 F2 F1 F0 * P 01 .....F.....P.....F0 ETX

b. Series 28 FPLA/FPRP


START OF TEXT
START OF DATA FIELD
OUTPUT OPTION ID
OUTPUT OPTION DATA
START OF DATA FIELD
TRANSITION TERM ID
1 SPACE (MANDATORY)
TRANSITION TERM NUMBER
START OF DATA FIELD
COMPLEMENT VARIABLE ID
COMPLEMENT VARIABLE DATA
START OF DATA FIELD
INPUT VARIABLE ID
VARIABLE DATA
START OF DATA FIELD
PRESENT STATE ID
PRESENT STATE DATA
STX * A PR/OE * T 00 * C C0 * I I15 I14 I13 I12 I11 I10 I9 I8 I7 I6 I5 I4 I3 I2 I1 I0 * P P5 P4 P3 P2 P1 P0
START OF DATA FIELD
NEXT STATE ID
NEXT STATE DATA
START OF DATA FIELD
OUTPUT ID
OUTPUT DATA
DATA FOR ALL TERMS USED
END OF TEXT
* N N5 N4 N3 N2 N1 N0 * F F7 F6 F5 F4 F3 F2 F1 F0 * T 01.....*C.....*I.....*P.....*N.....*F.....F0 ETX

c. Series 28 FPLS

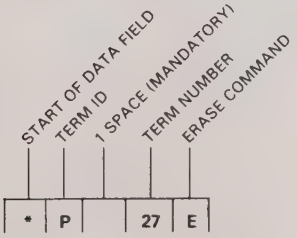
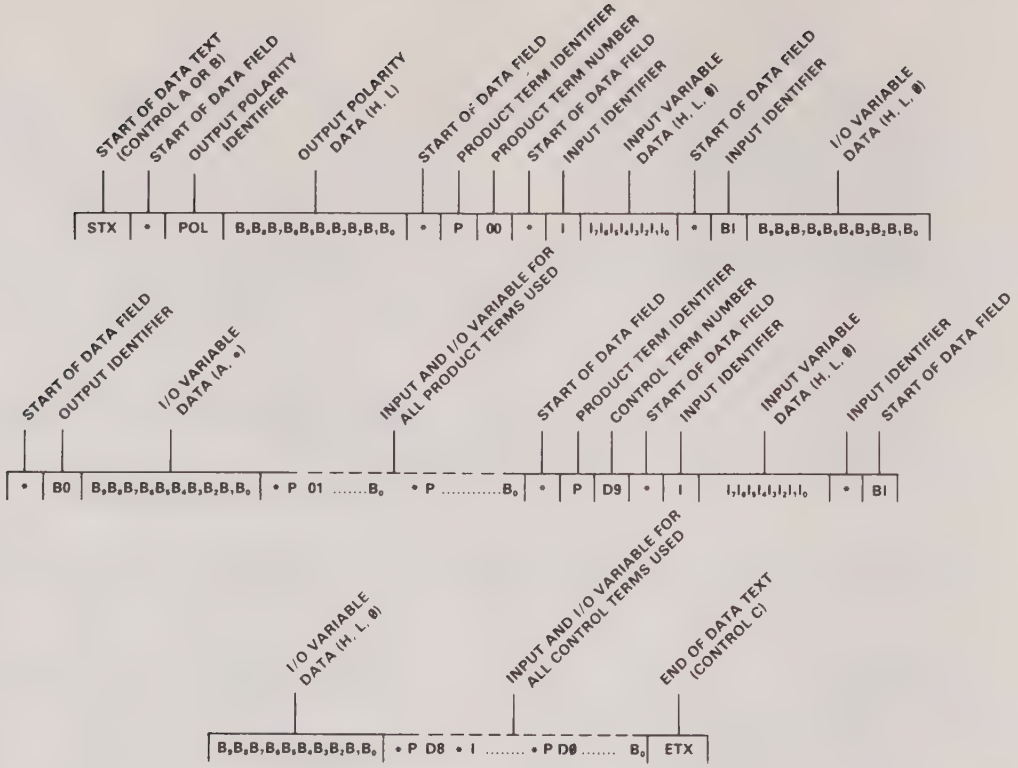


Figure 3-13. Input Data Stream Format



d. Series 20 FPLA

Figure 3-13. (Continued)

asterisk and a letter. Tables 3-8 through 3-10 list and describe the valid states and ID codes for each device.

Term numbers may appear in any order. Within each term, all fields must appear in the order described for each device.

To erase an entry, follow it with a backspace and a rubout. To erase an entire term's entries, enter the ID code, one space, the term number, and the letter E.

NOTE

The programmer has no timeout (normally 25 seconds) when inputting data in the E2 input mode. Take your time.

SERIES 28 FPGA. Table 3-8 lists the valid states and field ID codes for this device.

Table 3-8. Series 28 FPGA ID Codes and Logic Entry

Entry	Gate ID = *G (Gate Number)	
	Output Active Level ID = *A	Input Array ID = *I
H	HIGH	TRUE
L	LOW	FALSE
-	NA	DON'T CARE
Ø	NA	INACTIVE

1. Invoke Select Code E2.
2. Enter CTL A or CTL B.
3. Enter *G, exactly one space, and a gate number. Gates do not have to appear in numerical order, but each gate must include both fields of varibles (steps 4 through 7).
4. Enter *A.
5. Enter the Output Active Level for this gate.
6. Enter *I.
7. Enter all 16 of the Input Array variables starting with the highest-numbered input.
8. Repeat steps 3 through 7 until you've entered all of your function table.
9. Enter CTL C.
10. Insert a blank device in the socket adapter and start a Program operation.

SERIES 28 FPLA/FPRP. Table 3-9 lists the valid states and field ID codes for this device.

Table 3-9. Series 28 FPLA/FPRP ID Codes and Logic Entries

ENTRY	FPLA OUTPUT ACTIVE LEVEL ID = *A	TERM ID = *P (TERM NUMBER)	
		INPUT ARRAY ID = *I	OUTPUT ARRAY ID = F*
H	HIGH	TRUE	NA
L	LOW	FALSE	NA
-	NA	DON'T CARE	NA
Ø	NA	INACTIVE	NA
A	NA	NA	ACTIVE
●	NA	NA	INACTIVE

1. Invoke Select Code E2.
2. Enter CTL A or CTL B.
3. Enter *A.
4. Enter states for all eight of the Output Active Level Array variables starting with the highest-numbered output.

NOTE

For programming a Series 28 FPRP, enter H (Active High) for all of the Output Active Levels.

5. Enter *P, exactly one space, and a product term number. Product terms do not have to appear in numerical order, but each must include both fields of variables (steps 6 through 9).
6. Enter *I.
7. Enter states for all 16 Input Array variables, starting with the highest-numbered input.
8. Enter *F.
9. Enter the states for all eight of the Output Array variables, starting with the highest-numbered output.
10. Repeat steps 5 through 9 until you've entered all of your function table.
11. Enter CTL C.
12. Insert a blank device in the socket adapter and start a Program operation.

SERIES 28 FPLS. Table 3-10 lists the valid state entries and field ID codes for SERIES 28 serieal input.

1. Invoke Select Code E2.
2. Enter CTL A or CTL B.
3. Enter *A.
4. Enter a character to set the PR/$\overline{OE}$ option to its desired state.

Table 3-10. Series 28 FPLS ID Codes and Logic Entry

ENTRY	PR/$\overline{OE}$ ID = *A	TERM ID = *T (TERM NUMBER)		
		COMPLEMENT ARRAY ID = *C	INPUT & PRESET STATE ARRAYS ID = *I & *P	NEXT STATE & OUTPUT ARRAYS ID = *N & *F
H	PRESET	NA	TRUE	SET
L	OUTPUT ENABLE	NA	FALSE	RESET
-	NA	TRANSPARENT	DON'T CARE	NO CHANGE
Ø	NA	INACTIVE	INACTIVE	INACTIVE
A	NA	GENERATE	NA	NA
●	NA	PROPAGATE	NA	NA

5. Enter *T, exactly one space and a transition term number. Transition terms do not have to appear in numerical order, but each must include all five fields of variables (steps 6 through 15).

6. Enter *C.

7. Enter a state for the Complement Array variable.

8. Enter *I.

9. Enter states for all 16 of the Input Array variables with the highest-numbered input first.

10. Enter *P.

11. Enter states for all six of the Present State Array variables with the highest-numbered variable first.

12. Enter *N.

13. Enter states for all six of the Next State Array variables with the highest-numbered variable appearing first.

14. Enter *F.

15. Enter states for all six of the Next State Array variables with the highest-numbered variable appearing first.

16. Repeat steps 5 through 15 until you've entered the entire function table.

17. Enter CTL C.

18. Insert a blank device in the socket adapter and start a Program operation.

SERIES 20 FPLA. Table 3-11 lists the valid state entries for the Series 20 FPLA input.

1. Invoke Select Code E2.

2. Enter CTL A or CTL B.

3. Enter *POL.

4. Enter states for all ten of the output polarity array variables starting with the highest numbered output.

5. Enter *P and a product term number. Product terms do not have to appear in numerical order, but each product term must include all the fields of variables (steps 6 through 11).

6. Enter *I.

7. Enter states for all eight input array variables, starting with the highest numbered input.

8. Enter *BI.

9. Enter states for all ten B(I) input array variables, starting with the highest numbered input.

10. Enter *BO (only for terms Ø through 31).

11. Enter states for all ten B(O) output array variables, starting with the highest numbered output (only for terms Ø through 31).

12. Repeat steps 5 through 11 until you have entered all of your function table.

13. Enter CTL C.

14. Insert a blank device in the socket adapter and start a Program operation.

3.6.2 OUTPUT

Use E3 to output Signetics logic data. Install the Logic Pak and the proper socket adapter before you invoke the output command.

When outputting to a CRT terminal, you can interrupt the output to examine the display by entering CTL S. Restart the output by entering CTL Q.

Figure 3-14 illustrates the output formats for the different IFL devices.

3.7 VERIFY

The Verify mode is useful for checking the integrity of a Program or Load operation. Verify errors can be displayed either on the terminal or on the System 19's front panel display.

3.7.1 TERMINAL VERIFY

To display verify errors on the screen:

- From the System 19 Keyboard, press:
  SELECT
  E1
  START

- On a terminal, enter:
  E
  4

The terminal displays errors as pairs of lines of information. The top line of each pair will be the logic states stored in RAM, while the lower line is logic states programmed in the device for the same term or gate. See Figure 3-15.

NOTE

Use CTL S to interrupt Verify Output and CTL Q to resume output to the terminal.

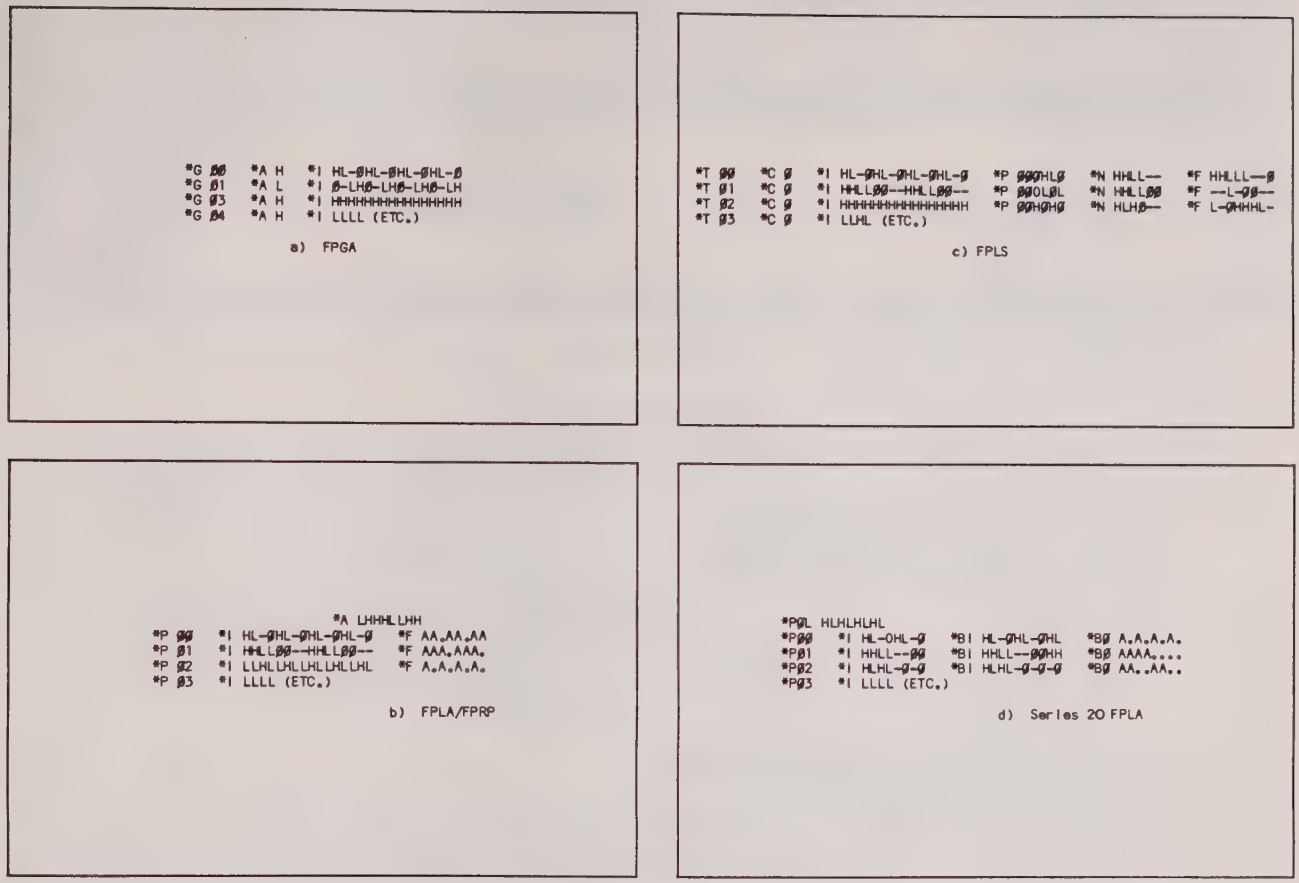

*G ØØ *A H *I HL-ØHL-ØHL-ØHL-Ø
*G Ø1 *A L *I Ø-LHØ-LHØ-LHØ-LH
*G Ø3 *A H *I HHHHHHHHHHHHHHHH
*G Ø4 *A H *I LLLL (ETC.)
a) FPGA
*T ØØ *C Ø *I HL-ØHL-ØHL-ØHL-Ø *P ØØØHLØ *N HHLL-- *F HHLLL--Ø
*T Ø1 *C Ø *I HHLLØØ--HHLLØØ-- *P ØØOLØL *N HHLLØØ *F --L-Ø-Ø--
*T Ø2 *C Ø *I HHHHHHHHHHHHHHHH *P ØØHØHØ *N HLHØ-- *F L-ØHHHL-
*T Ø3 *C Ø *I LLHL (ETC.)
c) FPLS
*A LHHHLLHH
*P ØØ *I HL-ØHL-ØHL-ØHL-Ø *F AA.AA.AA
*P Ø1 *I HHLLØØ--HHLLØØ-- *F AAA.AAA.
*P Ø2 *I LLHLLHLLHLLHLLHL *F A.A.A.A.
*P Ø3 *I LLLL (ETC.)
b) FPLA/FPRP
*PØL HLHLHLHL
*PØØ *I HL-OHL-Ø *BI HL-ØHL-ØHL *BØ A.A.A.A.
*PØ1 *I HHLL--ØØ *BI HHLL--ØØHH *BØ AAAA....
*PØ2 *I HLHL-Ø-Ø *BI HLHL-Ø-Ø-Ø *BØ AA..AA..
*PØ3 *I LLLL (ETC.)
d) Series 20 FPLA

Figure 3-14. Output Formats

3.7.2 FRONT PANEL VERIFY

Programmed logic devices can be verified from the front panel for your programmer according to the instructions in your programmer manual. Any errors will be given as hex data.

Errors can be given as logic variables if you are using a System 19. The key sequence for this special front panel verify is:

- Press:

  SELECT
  EØ
  ENTER (3 times)
  VER
  START

Table 3-11. Series 20 FPLA Codes and Logic Entry

ENTRY	ACTIVE LEVEL ID = *POL	TERM ID = *P (TERM NUMBER)		
		INPUT ARRAY ID = *I	BIDIRECTIONAL INPUT ARRAY ID = *BI	BIDIRECTIONAL OUTPUT ARRAY ID = *BO
H	HIGH	TRUE	TRUE	NA
L	LOW	FALSE	FALSE	NA
-	NA	DON'T CARE	DON'T CARE	NA
Ø	NA	INACTIVE	INACTIVE	NA
A	NA	NA	NA	ACTIVE
0	NA	NA	NA	INACTIVE

Press and hold DEVICE DATA. The flashing will stop and the display will contain the logic state at the same location in the device.

If a misverify occurs, the programmer will halt and the display will flash on and off with RAM data (term number, field number, variable number, and logic state).

NOTE

This feature can be used only on the System 19.

3.8 ERROR CODES

Table 3-12 lists the Logic Pak error codes. Other error codes will appear depending on the programmer you are using. These are listed in the programmer manual.

Table 3-12. Error Codes

CODE	DESCRIPTION	CODE	DESCRIPTION
22	The programming electronics were unable to program the device; or with Series 28 FPRP only, you attempted to program non-existent Output Active-Level fuses.	33	A programming module writer error detected; the scratch RAM failed a write-read test.
31	The programmer aborted during an operation due to excessive current drain.	38	Calibration error: the test number may be out of range, you attempted to program while in the calibration mode, or you attempted to enter step 27 with a Series 28 FPGA socket adapter installed.
32	The programmer aborted due to excessive current drain during a backwards device test. The device may be in the socket backwards.		

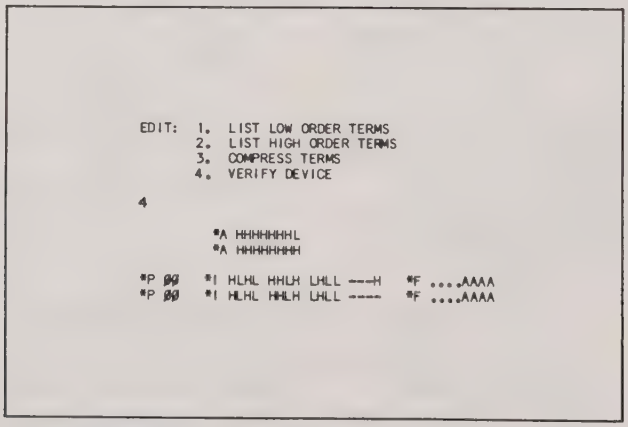

EDIT: 1. LIST LOW ORDER TERMS
2. LIST HIGH ORDER TERMS
3. COMPRESS TERMS
4. VERIFY DEVICE
4
*A HHHHHHHHL
*A HHHHHHHHH
*P 00 *I HLHL HHLH LHLL ---H *F ....AAAA
*P 00 *I HLHL HHLH LHLL ---- *F ....AAAA

Figure 3-15. CRT Display for Misverified Logic

DATA I/O

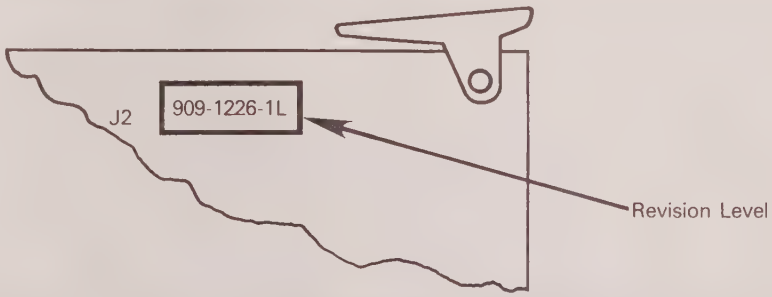
Field Bulletin

To: All MMI PROM and PAL Users
Subject: Specification Changes

July, 1982
FB #021-0202

Currently being Updated at Data I/O 1427
1226's need to be done.

This Field Bulletin affects Personality Card Sets 909-1226-1 Revision "L" and earlier, 909-1515-1 Revision "B" and earlier, and 909-1427-1 Revision "G" and earlier. To identify the card set and revision level, check the label attached to the J2 connector on the Analog Card.



The program/verify algorithm for the MMI Generic PROMs and PALs has changed. To insure the highest possible yields, it is recommended that the above listed card sets be updated to the latest specifications.

The following is a summary of the changes for each card set:

1. **909-1226-1 L (Generic PROM Family #1 Card Set)**
   The pulse width (TPW) of the "Bit To Program" waveform has changed from 7 ± 5 microseconds to 15 +10/−5 microseconds. To update your card set to the latest specification, replace the Timing Diagram in your manual with the one enclosed (007-1226-1), and recalibrate the card set per the instructions in your manual. To set TPW to the new value, adjust R5 on the Digital Card. If recalibration is not convenient, or if your card set is Revision Level "F" or earlier, contact the nearest Data I/O Service Center for assistance.
2. **909-1515-1 B (Generic PROM Family #2 Card Set)**
   The V_{CC} voltage during one of the verify cycles (V_{CCVF}) has increased from 4.0 ± 0.1 volts to 4.3 ± 0.1 volts. To update your card set to the latest specification, recalibrate the card set using the enclosed Calibration Chart (017-1515-1), paying particular attention to Step 4-4. If recalibration is not convenient, contact the nearest Data I/O Service Center for assistance.
3. **909-1427-1 G (PAL Program Card Set)**
   The V_{CCP} and V_{HH} voltage has increased from 11 ± 0.5 volts to 11.5 ± 0.5 volts. To update the card set to the latest specification, recalibrate using the enclosed Calibration Chart (017-1427-1), paying particular attention to Steps 2-1 and 4-1. If recalibration is inconvenient, contact the nearest Data I/O Service Center for assistance.

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DATA I/O

Field Bulletin

To: All Signetics IFL Users
(Integrated Fuse Logic)
Subject: New Programming Specifications

July, 1982
FB #021-0204

This Field Bulletin affects the following Logic Programming Paks:

919-1542 All Revisions
950-0800 All Revisions
919-0045 Rev "B" and Earlier
950-0104 Rev "B" and Earlier

Signetics has changed the Programming Algorithm for their IFL Family of devices. To comply with this change and insure the highest possible yields, the Programming Paks listed above must be updated. These updates can be accomplished by any of the service centers listed at the end of this bulletin.

If your Pak is a 919-1542 or 950-0800, it will be updated to a 919-0045-002C on 950-0104-002C. This part number change reflects not only the latest algorithm, but also the new memory map for storing fuse data in RAM. The reason for the new memory map is to make it compatible with the new 20-pin devices being released and the new JEDEC Translation Format for programmable logic device data transfer. Because of this memory map change, it will be necessary for you to store your logic data patterns in a master device or in the serial I/O logic format (select E2) onto paper tape or some other storage medium, so that when you receive your updated pak the data can be loaded into RAM properly.

NOTE TO FPRP (82S106, 82S107) USERS:

After your Pak has been modified to the new specification it will no longer support the FPRP devices. If you require the capability to program this device, notify the service center of this requirement when you return your Pak for updating. They will install special rework to accomodate this device.

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SECTION 4
TROUBLESHOOTING AND CALIBRATION

4.1 INTRODUCTION

The following information is an aid to interpreting malfunctions and locating hardware failures in the Logic Pak. System failures can be divided into two categories:

- No system operation
- Persistent or intermittent test-stage errors (or poor yields)

These categories, covered in paragraphs 4.2 and 4.3, will direct the service technician to the portion of the circuitry implicated by test errors or unacceptable calibration results. Table 4-1 can be used to isolate the problem to a suspect board or component. Section 5, Circuit Description, and Appendix C, Schematics, may provide additional information useful in troubleshooting.

After successful troubleshooting, perform a complete calibration of the Logic Pak, as described in Section 4.4.

4.2 NO SYSTEM OPERATION

Perform the following steps if the system will not operate after installation of the Logic Pak. After completing each step, determine whether the problem still exists.

1. Check for proper installation of the Logic Pak (refer to Section 2).

2. Check all cables for proper insertion and orientation. Check the Logic Pak-to-programmer connector for bent pins.

3. Check power supplies (refer to section 4.4)

Table 4-1. Troubleshooting Components

TEST NUMBER	SUSPECT BOARDS	SUSPECT COMPONENTS
1-5	701-1542	Q18, Q25, U1, U11, U12
6-12	701-1598	CR1, Q2, Q3, U1-U9, VR1
13-16	701-1542	Q1, Q3, Q6-Q13, U2, U3, U6-U9, U13, U14
17-18	701-1542	Q16, Q17, U12, VR1
19	701-1542	Q23, U1
20-22	701-1542	A3, Q1, Q16, Q17, U12, VR1
23	701-1542	Q23, U11
24	701-1542	Q4, Q19, VR2
25	701-1542	U4-U10
26-27	701-1542	CR2, CR3, CR4, CR7, Q14, Q15, U12
28-30	701-1598	U5
31	701-1542	Q20, Q21, Q22, Q25, U1
32	701-1598	Q5-Q8, U1
33-34	701-1542	Q20, Q21, Q22, Q24, U11
35	701-1542	CR17, Q10, Q24, U11

4. If steps 1 to 3 do not reveal the problem, contact your local Data I/O Service Center.

4.3 PERSISTENT OR INTERMITTENT TEST-STAGE ERRORS

Perform the following steps to isolate a system failure. After completing each step, determine whether the problem still exists.

1. Substitute a good device to determine if a hardware problem exists.

2. Check for proper installation of the Logic Pak (refer to Section 2).

3. Check all cables for proper insertion and orientation. Check the Logic Pak-to-programmer connector for bent pins.

4. Perform a complete calibration. Note any voltages still falling outside the indicated limits, and then refer to the corresponding test number in Table 4-1 to locate the suspect board or component. Referring to the circuit description and schematics may also prove helpful.

5. Perform waveform observation tests. Note any waveform irregularities. Referring to the circuit description (Section 6) and the schematic (Appendix C) may prove helpful in determining the cause of any irregularities.

6. If steps 1 to 5 do not reveal the problem, contact your local Data I/O Service Center.

4.4 CALIBRATION

Data I/O suggests that you calibrate the Logic Pak whenever programming yields fall below Signetics' recommended minimums or after troubleshooting.

NOTE

Calibration can only be done on a programmer with an address and data display.

Calibration consists of three parts:

1. **Power Supply Calibration.** These are measurements of the DC supply voltages of the programmer. All other voltages depend on these supplies; therefore, this step must be done first.

2. **DC Calibration.** This consists of measuring and adjusting other critical DC voltage levels generated by the Logic Pak.

3. **Waveform Observation**. Programming waveforms can be observed on an oscilloscope for compliance with Signetics' critical voltage and timing specifications.

Because of the different possible combinations of programmers and programming modules this manual does not attempt to cover all areas of calibration. Instead, it lists the steps necessary to calibrate the Logic Pak. For information on how to carry out these steps on the various programmers, consult your programmer manual.

4.4.1 REQUIRED EQUIPMENT

- Programmer (with display)
- Data I/O Calibration Extender
- Digital Voltmeter (Fluke 8000A or equivalent)
- Dual-trace Oscilloscope (Tektronix 465 or equivalent)
- IFL Socket Adapter(s)

4.4.2 POWER SUPPLY CALIBRATION

Follow the procedure for power supply measurements in the appropriate programmer manual.

4.4.3 EQUIPMENT SET-UP

Install the Calibration Extender, Logic Pak and socket adapter as follows. Refer to Figure 4-1:

1. Turn the power off.

2. Remove the Logic Pak from the programmer by gently pulling the handle to separate the mating connectors, and then lifting it out.

3. Disassemble the Logic Pak as described in Section 2.2.

4. Install the Calibration Extender just as you would the Logic Pak, being sure to seat it in the programmer's mating connector.

5. Insert the Logic Pak's 64-pin connector in the connector on the Calibration Extender. The socket can then be most easily probed if the top assembly is hooked over the lip of the card cage and laid across the programmer.

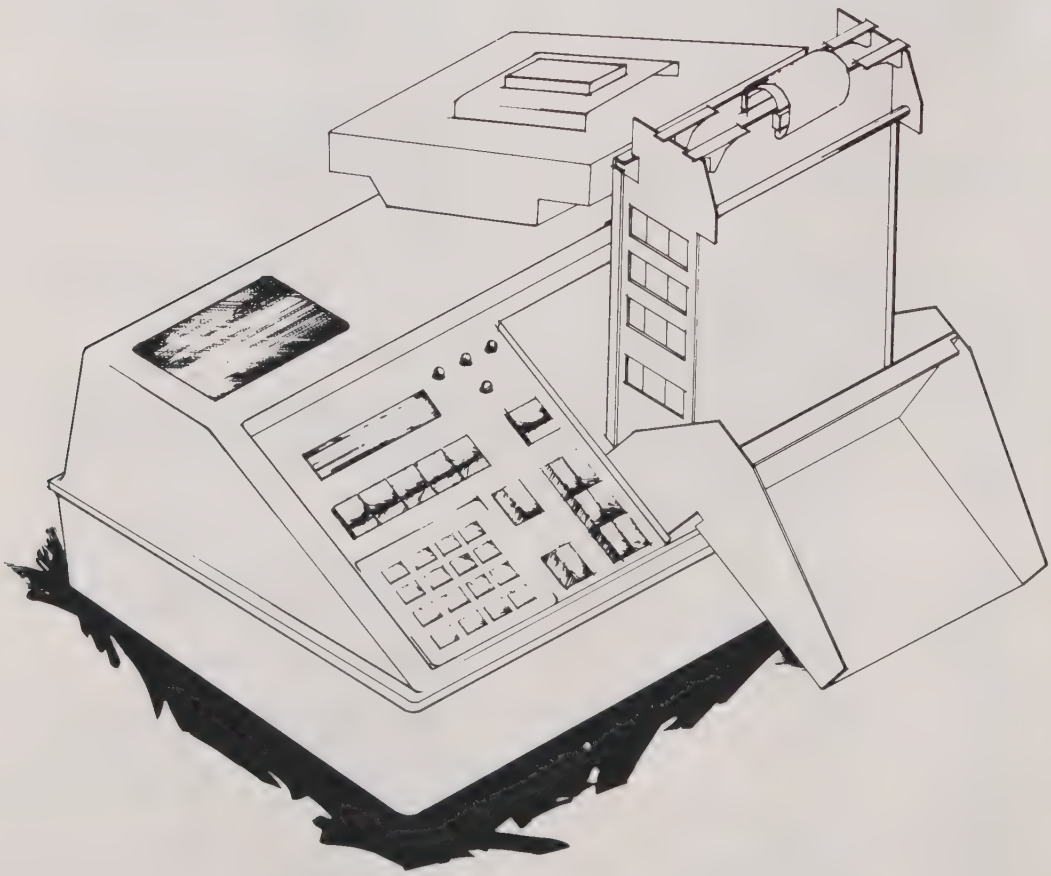


Figure 4-1. Logic Programming Pak Prepared for Calibration

6. Install an IFL socket adapter.

NOTE

The socket adapter tells the programming module which voltage and waveforms to generate. The Measurement Chart and Timing Diagrams specify which socket adapter each calibration test is for. With no socket adapter installed, Series 20 FPLA waveforms are generated and calibration may be performed as if the 715-0018-001 socket adapter were installed. Reselect the calibration mode anytime the socket adapter is changed.

4.4.4 THE MEASUREMENT CHART

The Measurement Chart presents the information you need for all AC and DC tests. Each step is presented as follows:

- The STEP column tells which step number to use for each test. Step numbers are set at the programmer keyboard.
- The TEST NO. column identifies the individual tests.
- The TEST DESCRIPTION column explains the function being tested.
- The TEST POINT(S) column tells which pin(s) on the socket adapter to probe for measuring voltages.
- The VOLTAGE columns specify the voltage limits. If a reading falls outside the range and cannot be brought into range, the Logic Pak should not be used until the condition is corrected.
- The ADJUST LOCATION column tells which potentiometer (if any) to adjust if a voltage is out of tange.
- The COMMENTS column gives special instructions for particular tests.

4.4.5 KEY SEQUENCES FOR CALIBRATION

Consult your programmer manual for the appropriate key sequences for entering and exiting the calibration mode. Perform each Measurement Chart step in order. If adjustments are required, refer to Figure 4-2 to locate the potentiometers.

4.4.6 WAVEFORM OBSERVATION

Waveform observation steps follow DC calibration steps on the Measurement Charts.

With the correct Measurement Chart step selected, compare the waveform displayed on the oscilloscope with the Timing Diagram waveform called out in the COMMENTS column of the Measurement Chart.

NOTE

The programmer does not increment through the waveform observation steps. To reach each step, exit and re-enter the calibration mode.

Measurement Chart

PROGRAMMING MODULE 950-0104
PERFORMANCE BOARD NA
SOCKET ADAPTER 715-1594-1, 715-1594-2
715-1595

DATE	REV	REVISION RECORD	DR	CK
12-7-81	A	Release	WT.	GL

STEP	TEST NO.	TEST DESCRIPTION	TEST LOCATION		VOLTAGES			ADJUSTMENT LOCATION	COMMENTS
			Pin Number	SOCKET ADAPTER	MIN	NOM	MAX		Ground DVM on socket pin 14.
1	1	VCC PROGRAM/VCCL	28	715-1594-1 or -2	-0.4	NA	0.8	NA	
2	2	VCC VERIFY/VH	28	"	5.40	5.50	5.60	R52,701-1542	Insert 100Ω, 1W, pin 28 to pin 14.
3	3	VCC VERIFY/VL	28	"	4.40	4.50	4.60	R53, "	" "
4	4	VCC PROGRAM/VCCP	28	"	4.75	5.00	5.25	R54, "	" "
5	5	VCC PROGRAM/VCCS	28	"	8.25	8.50	8.74	R51, "	" "
6	6	VIHH GENERATOR	3	"	9.50	10.1	10.5	R4, 701-1598	Insert 1KΩ, ¼W, pin 3 to pin 14; see note 1.
6	7	EVEN ADDRESS/VIHH	3,5,7,9,21,23,25,27	"	9.50	NA	10.5	NA	
7	8	ODD ADDRESS/VIHH	2,4,6,8,20,22,24,26	"	9.50	"	10.5	"	
8	9	ODD ADDRESS/VIL	2,4,6,8,20,22,24,26	"	0.0	"	0.4	"	
8	10	EVEN ADDRESS/VIH	3,5,7,9,21,23,25,27	"	4.8	"	5.2	"	
9	11	EVEN ADDRESS/VIL	3,5,7,9,21,23,25,27	"	0.0	"	0.4	"	
9	12	ODD ADDRESS/VIH	2,4,6,8,20,22,24,26	"	4.8	"	5.2	"	
10	13	EVEN OUTPUT/VIH	10,12,15, 17	"	4.70	"	5.25	"	
10	14	ODD OUTPUT/VIL	11,13,16,18	"	0.0	"	0.4	"	
11	15	ODD OUTPUT/VIH	11,13,16,18	"	4.70	"	5.25	"	
11	16	EVEN OUTPUT/VIL	10,12,15,17	"	0.0	"	0.4	"	
12	17	VP GENERATOR	10	"	16.0	17.0	18.0	R3,701-1542	Insert 100 Ω, 3W, pin 10 to pin 14
									after selecting step 12, see note 2.
12	18	EVEN OUTPUT/PROG.	10,12,15,17	"	16.0	NA	18.0	NA	
12	19	NINTH OUTPUT FPGA/PROG.	9	715-1595 only	16.0	"	18.0	"	
12	20	ODD OUTPUT/VIH	11,13,16,18	715-1594-1 or 2	4.50	"	6.50	"	
13	21	ODD OUTPUT/PROG.	11,13,16,18	"	16.0	"	18.0	"	
13	22	EVEN OUTPUT/VIH	10,12,15,17	"	3.80	"	5.80	"	

NOTES:
1. ERROR 31, OVERCURRENT, FLAGGED IF ATTEMPT IS MADE TO ADJUST THE VIHH GENERATOR GREATER THAN 16 V
2. ERROR 31, OVERCURRENT, FLAGGED IF VP GENERATOR IS ADJUSTED 0.7 V BELOW VOP-GENERATOR VALUE.

Measurement Chart

PROGRAMMING MODULE 950-0104
PERFORMANCE BOARD NA
SOCKET ADAPTER 715-1594-1, 715-1594-2, 715-1595

DATE	REV	REVISION RECORD	DR	CK
		See page 1	WF	GL

STEP	TEST NO.	TEST DESCRIPTION	TEST LOCATION	VOLTAGES MIN	VOLTAGES NOM	VOLTAGES MAX	ADJUSTMENT LOCATION	COMMENTS CAUTION: MOMENTARILY INSERT RESISTORS DURING STEPS 21 THRU 25.
13	23	NINTH OUTPUT FPGA/VIH	9 715-1595 ONLY	3.80	NA	5.80	NA	
14	24	VOP GENERATOR	18 715-1594-1 or 2	9.50	10.00	10.5	R29,701-1542	Insert 1KΩ, ¼W, pin 18 to pin 14, see note 2.
15	25	COMP/OUTPUT BUFFER	NA	NA	NA	NA	NA	Front panel: blink=fail, no blink =pass
16	26	VFF/VV	1 715-1594-1 or -2	1.25	"	1.75	"	
17	27	VFE/VOPH	1 "	16.0	"	18.0	"	
18	28	CS/VIL	19 "	0.0	"	0.4	"	
19	29	CS/VIH	19 "	4.8	"	5.2	"	CAUTION: DO NOT PERFORM STEPS 21-25
20	30	CS/VIHH	19 "	9.5	"	10.5	"	UNLESS ALL PREVIOUS STEPS VERIFY.
21	31	VCC/OVERCURRENT	NA "	NA	"	NA	"	Insert 7.5Ω, ¼W, pin 28 to pin 14,
								error code 31 displayed.
22	32	VIHH OVERCURRENT	" "	"	"	"	"	Insert 25Ω, ¼W, pin 19 to pin 14,
								error code 31 displayed.
23	33	VPP OVERCURRENT	" "	"	"	"	"	Insert 10Ω, ¼W, pin 1 to pin 14,
								error code 31 displayed.
24	34	VOP OVERCURRENT	" "	"	"	"	"	Insert 100Ω, ¼W, pin 18 to pin 14,
								error code 31 displayed.
25	35	BACKWARDS DEVICE	" "	"	"	"	"	Insert 10Ω, ¼W, pin 28 to pin 14,
								error code 32 displayed.
		WAVEFORM OBSERVATION						
26	36	FPGA AND ARRAY	715-1595					
28	37	FPGA OUTPUTPOLARITY	"					
26	38	FPLA AND ARRAY	715-1594-1					
27	39	FPLA OR ARRAY	"					

NOTES:

DATA I/O

Measurement Chart

PROGRAMMING MODULE 950-0104
PERFORMANCE BOARD
SOCKET ADAPTER 715-1594-1, 715-1594-2, 715-1595, 715-0018-001

DATE	REV	REVISION RECORD	DR	CK
		See page 1	WT.	GC

STEP	TEST NO.	TEST DESCRIPTION	TEST LOCATION	VOLTAGES MIN	VOLTAGES NOM	VOLTAGES MAX	ADJUSTMENT LOCATION	COMMENTS
28	40	FPLA OUTPUT POLARITY	715-1594-1					
26	41	FPLS AND ARRAY	715-1594-2					
27	42	FPLS OR ARRAY	"					
28	43	FPLS PR/OE OPTION	"					
29	44	ABORT CHECK	715-1594-1					Observe program pulse reject number as called out on Timing Diagram; front panel should blink.

NOTES:

Measurement Chart

PROGRAMMING MODULE 950-0104
PERFORMANCE BOARD NA
SOCKET ADAPTER 715-0018-001

DATE	REV	REVISION RECORD	DR	CK
		See page 1.	WT.	GL

STEP	TEST NO.	TEST DESCRIPTION	TEST LOCATION TEST POINT(S) PIN NUMBER	SOCKET ADAPTER	VOLTAGES MIN	NOM	MAX	ADJUSTMENT LOCATION	COMMENTS
									GROUND DVM ON SOCKET PIN 14.
1	1	VCC PROGRAM/VCCL	20	715-0018-001	-0.4	NA	0.8	NA	
2	2	VCC VERIFY/VH	20	"	5.40	5.50	5.60	R52701-1542	Insert 100Ω, 1W, pin 20 to pin 10.
3	3	VCC VERIFY/VL	20	"	4.40	4.50	4.60	R53 "	"
4	4	VCC PROGRAM/VCCP	20	"	4.75	5.00	5.25	R54 "	"
5	5	VCC PROGRAM/VCCS	20	"	8.25	8.50	8.75	R51 "	Insert 1KΩ, 1W, pin 20 to pin 10.
6	6	VIHH GENERATOR	19	"	9.50	10.1	10.5	R4,701-1598	Insert 1KΩ, ¼W, pin 19 to pin 10, see note 1.
6	7	EVEN ADDRESS/VIHH	2,4,6,8,12,14,17,19	"	9.50	"	10.5	"	
7	8	ODD ADDRESS/VIHH	1,3,5,7,9,11,13,15	"	9.50	"	10.5	"	
8	9	ODD ADDRESS/VIL	1,3,5,7,9,11,13,15	"	0.0	"	0.4	"	
8	10	EVEN ADDRESS/VIH	2,4,6,8,12,14,17,19	"	4.8	"	5.2	"	
9	11	EVEN ADDRESS/VIL	2,4,6,8,12,14,17,19	"	0.0	"	0.4	"	
9	12	ODD ADDRESS/VIH	1,3,5,7,9,11,13,15	"	4.8	"	5.2	"	
10	13	ODD OUTPUT/VIL	16	"	0.0	"	0.4	"	
11	14	ODD OUTPUT/VIH	16	"	4.70	"	5.25	"	
12	15	ODD OUTPUT/VIH	16	"	4.50	"	6.50	"	
13	16	ODD OUTPUT/PROG.	16	"	16.0	"	18.0	R3,701-1542	Insert 100Ω, 3W, pin 10 to pin 14 after selecting step 12. See note 2.

NOTES:
1. ERROR 31, OVERCURRENT, FLAGGED IF ATTEMPT IS MADE TO ADJUST THE VIHH GENERATOR GREATER THAN 16 V.
2. ERROR 31, OVERCURRENT, FLAGGED IF VP GENERATOR IS ADJUSTED 0.7 BELOW VOP-GENERATOR VALUE.

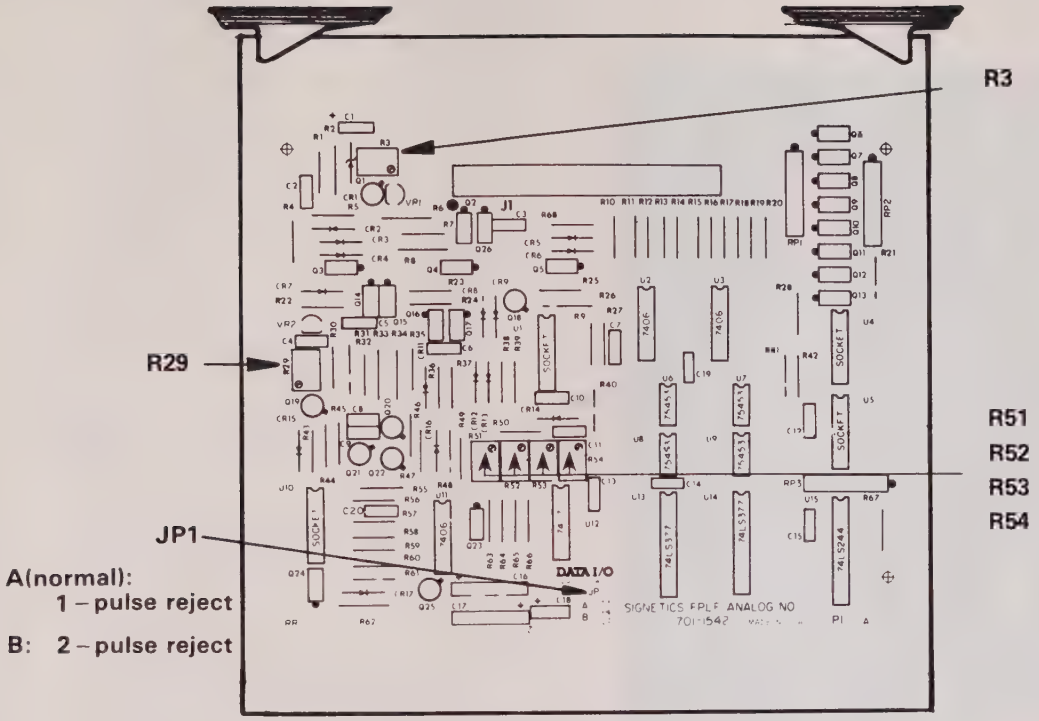
Measurement Chart

PROGRAMMING MODULE 950-0104
PERFORMANCE BOARD NA
SOCKET ADAPTER 715-0018-001

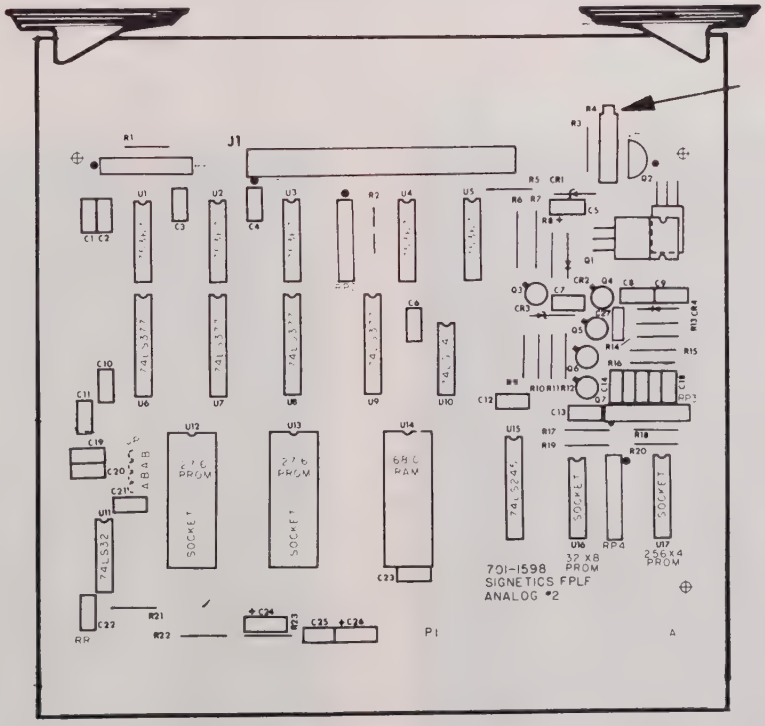
DATE	REV	REVISION RECORD	DR	CK
		See page 1	WT.	GL

STEP	TEST NO.	TEST DESCRIPTION	TEST LOCATION TEST POINT(S) PIN NUMBER	SOCKET ADATPER	VOLTAGES MIN	NOM	MAX	ADJUSTMENT LOCATION	COMMENTS CAUTION: MOMENTARILY INSERT RESISTORS DURING STEPS 21 THRU 25.
14	17	VOP GENERATOR	16	715-0018-001	9.5	10.0	10.5	R29701-1542	Insert 1KΩ, ¼W, pin 16 to pin 10, see note 2.
15	18	COMP/OUTPUT BUFFER	NA		NA	NA	NA	NA	Front panel: blink =fail, no blink=pass.
16	19	VFF/VV	18	715-0018-001	1.25	"	1.75	"	
17	20	VFE/VOPH	18	"	16.0	"	18.0	"	
21	21	VCC OVERCURRENT	NA	"	NA	"	NA	"	Insert 7.5Ω, ¼W, pin 20 to pin 10, error code 31 is displayed.
23	22	VPP OVERCURRENT	"	"	"	"	"	"	Insert 10Ω, ¼W, pin 18 to pin 10, error code 31 is displayed.
24	23	VOP OVERCURRENT	"	"	"	"	"	"	Insert 100Ω, ¼W, pin 16 to pin 10, error code 31 is displayed.
25	24	BACKWARDS DEVICE	"	"	"	"	"	"	Insert 10Ω, ¼W, pin 20 to pin 10, error code 32 is displayed.
			REFER TO TIMING DIAGRAM FOR TEST POINTS						
		WAVEFORM OBSERVATION							
26	25	AND ARRAY		"					
27	26	OR ARRAY		"					
28	27	OUTPUT POLARITY		"					

NOTES:
1. ERROR 31, OVERCURRENT, FLAGGED IF ATTEMPT IS MADE TO ADJUST THE VIHH GENERATOR GREATER THAN 16 V.
2. ERROR 31, OVERCURRENT, FLAGGED IS VP GENERATOR IS ADJUSTED 0.7 BELOW VOP-GENERATOR VALUE.

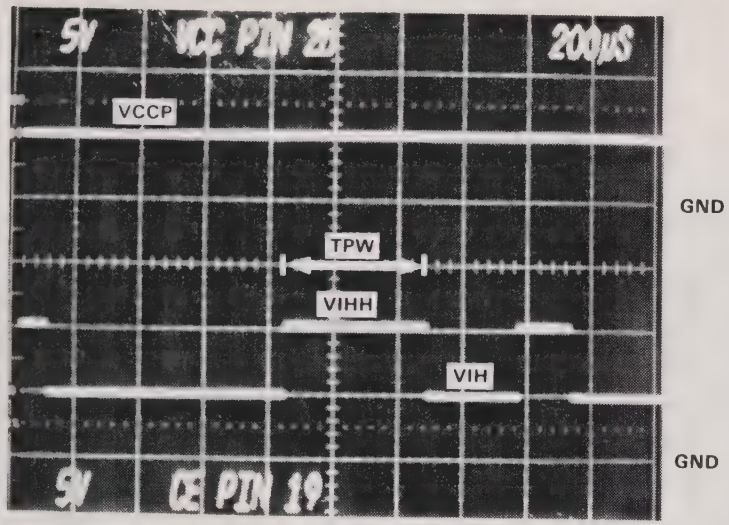


a) Analog Card #, 701-1542

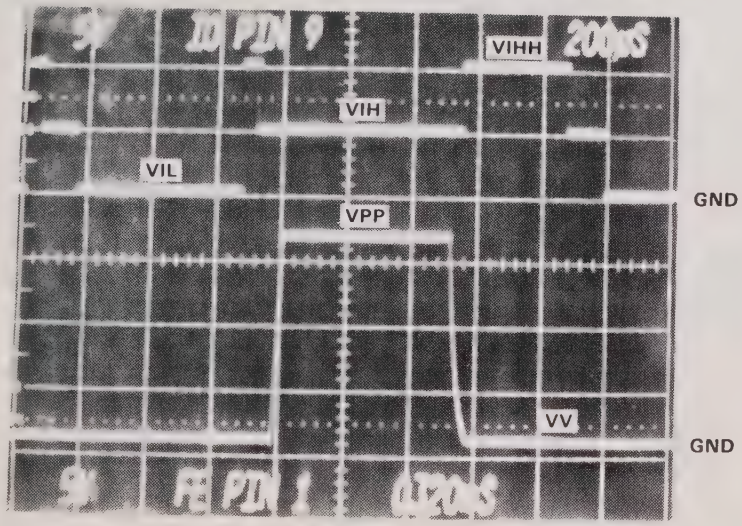


b) Analog Card #2, 701-1598

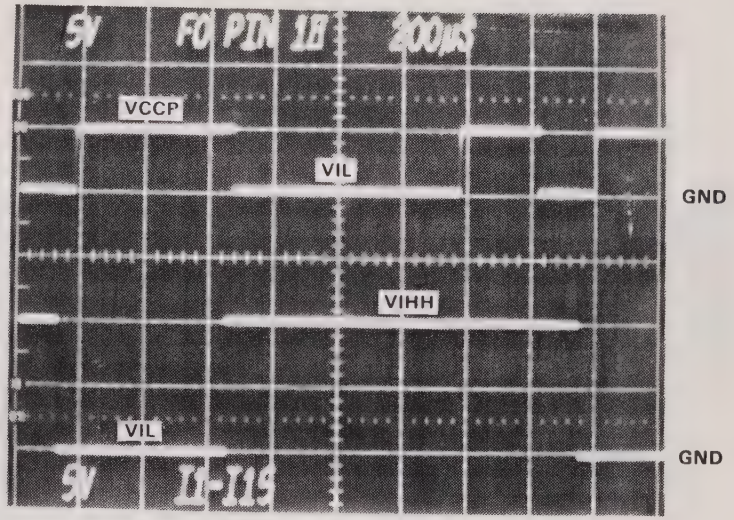
Figure 4-2. Adjustment Potentiometer and Jumper Locations


VCCP
GND
TPW
VIHH
VIH
GND

1


VIHH
VIH
VIL
GND
VPP
VV
GND

2


VCCP
VIL
GND
VIHH
VIL
GND

3

NOTES

1. *Oscilloscope trigger: Pin 18 of socket adapter 715-1594-1. Trigger on the positive slope. DC coupled.*

2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT

3. *Select calibration step 26.*

4. *Load Vcc with 100 ohm, 1 watt resistor.*

5. *Fill data RAM with hex data FF.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10	—	50	us	

REVISIONS

ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT	1/25/82

DATA I/O ISSAQUAH, WA

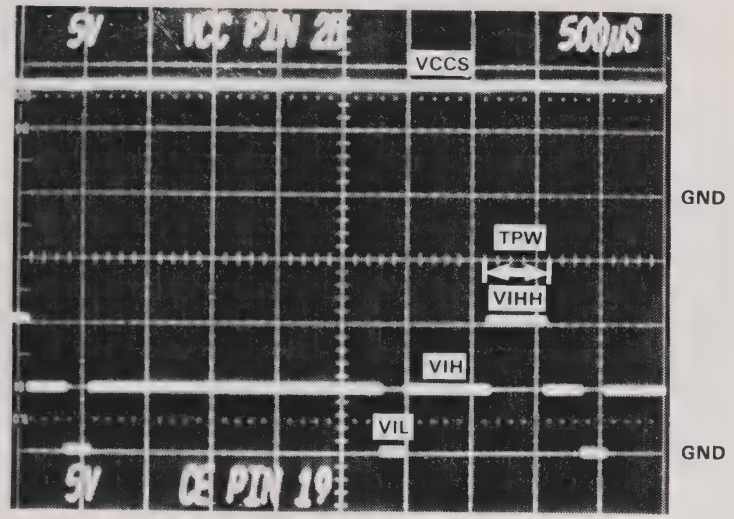
TITLE
TIMING DIAGRAM
SIGNETICS IFL
FPLA AND ARRAY

DRAWN BY: FD

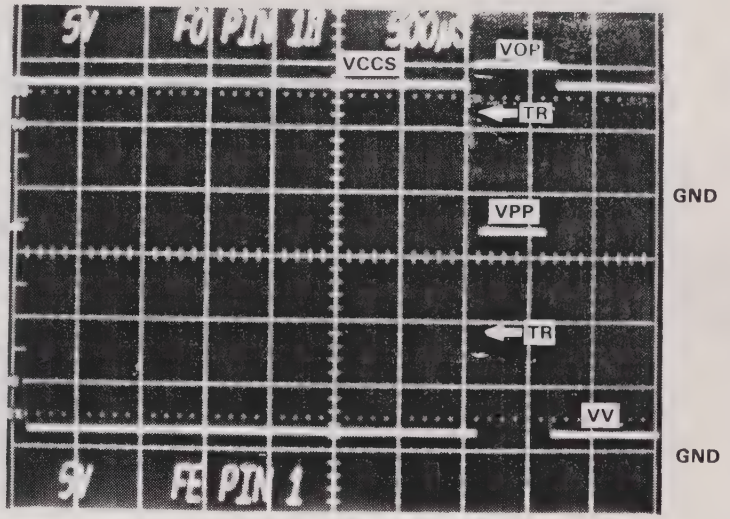
CHECKED BY: GL

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	34-950-0104

SCALE | SHEET 1/1


5V
VCC PIN 28
500µS
VCCS
GND
TPW
VIHH
VIH
VIL
GND
5V
CE PIN 19

1


5V
FO PIN 11
VCCS
VOP
TR
GND
VPP
TR
VV
GND
5V
FE PIN 1

2

NOTES

1. *Oscilloscope trigger: Pin 19 of socket adapter 715-1594-1. Trigger on the positive slope. DC coupled.*
2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT
3. *Select calibration step 27.*
4. *Load Vcc with 100 ohm, 1 watt resistor.*
5. *Fill data RAM with hex data FF.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10		50	us	

REVISIONS

ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT.	1/27/82

DATA I/O ISSAQUAH, WA

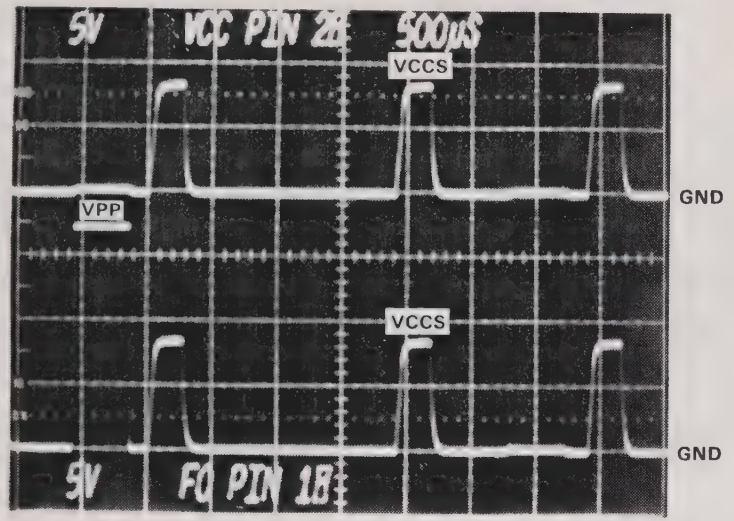
TITLE: TIMING DIAGRAM SIGNETICS IFL FPLA OR ARRAY

DRAWN BY: LJ

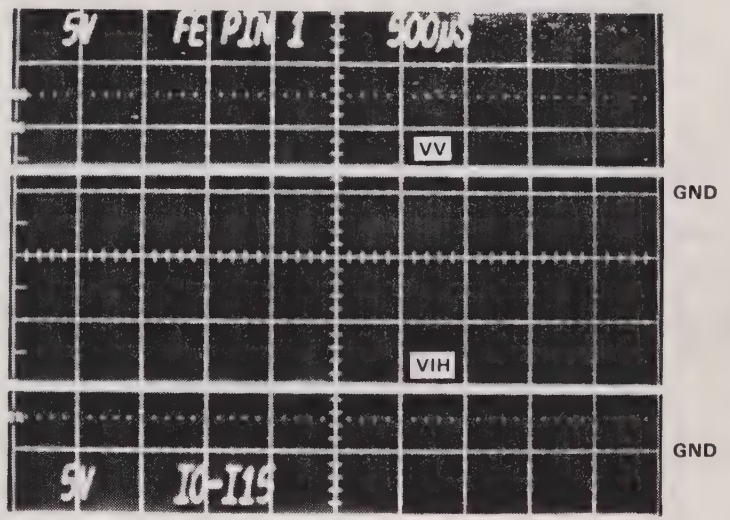
CHECKED BY: GC

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	34-950-0104

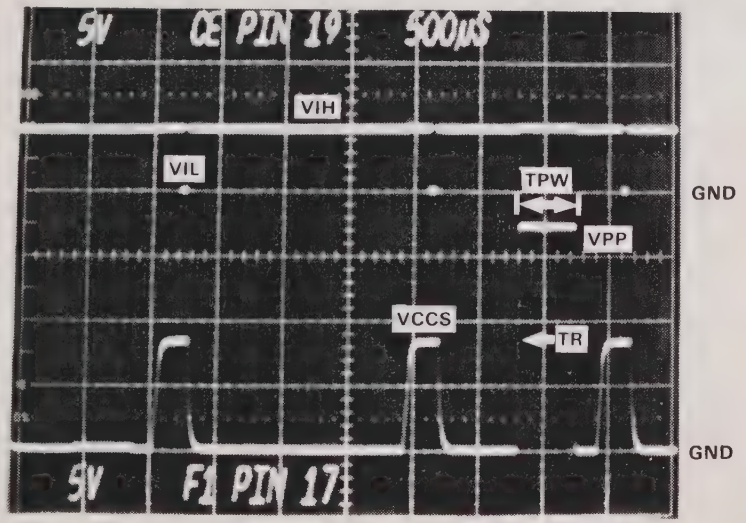
SCALE | SHEET 1/1


5V
VCC PIN 2
500µS
VCCS
VPP
GND
VCCS
GND
5V
FO PIN 18

1


5V
FE PIN 1
500µS
VV
GND
VIH
GND
5V
IO-I19

3


5V
CE PIN 19
500µS
VIH
VIL
TPW
GND
VPP
VCCS
TR
GND
5V
F1 PIN 17

2

NOTES

1. *Oscilloscope trigger: Pin 18 of socket adapter 715-1594-1. Trigger on the positive slope. DC coupled.*
2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT
3. *Select calibration step 28.*
4. *Load Vcc with 100 ohm, 1 watt resistor.*
5. *Fill data RAM with hex data FF.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10	—	50	us	

REVISIONS

ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT.	1/25/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
SIGNETICS IFL
FPLA OUTPUT POLARITY

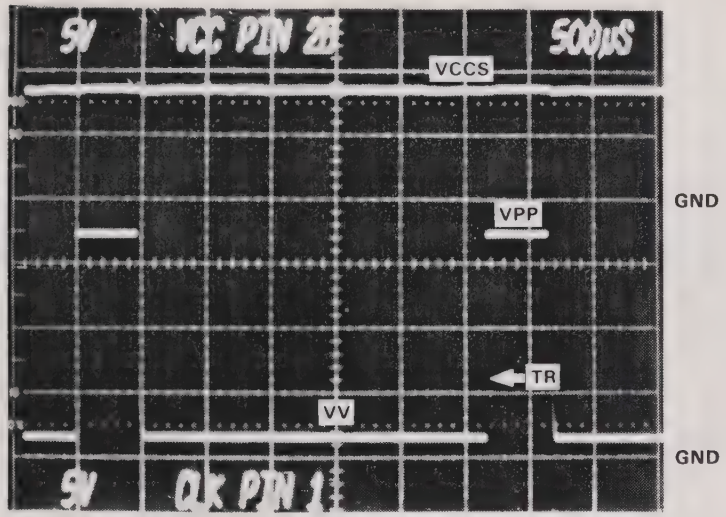
DRAWN BY: LJ.

CHECKED BY: GC

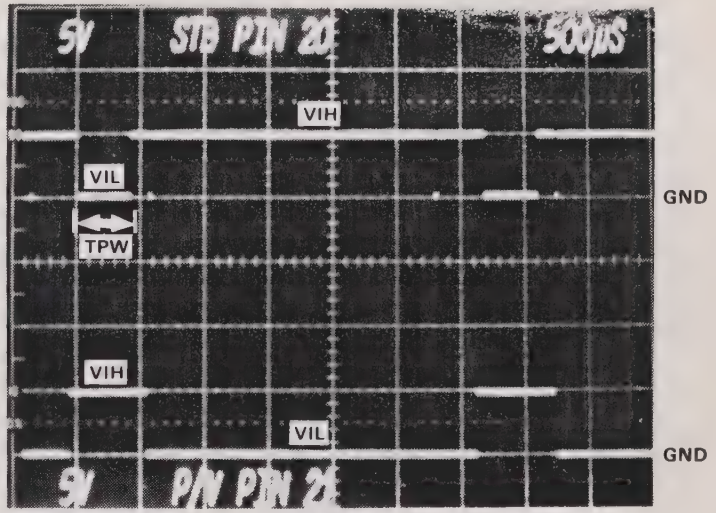
SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	34-950-0104

SCALE

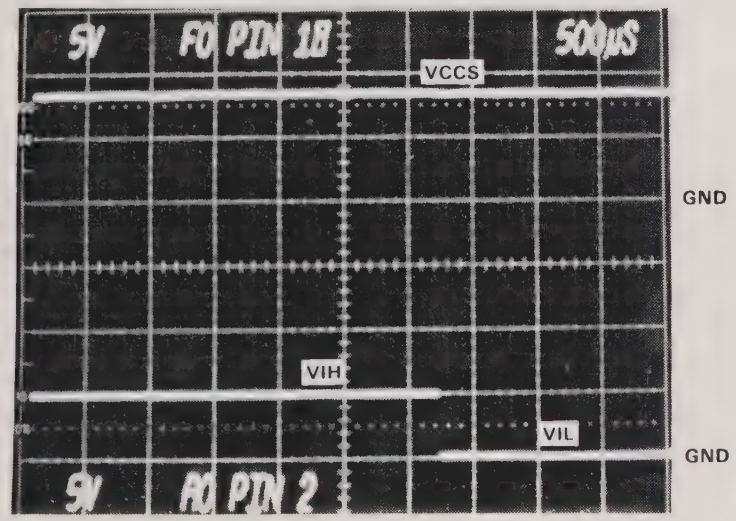
SHEET 1/1


5V
VCC PIN 2
500µS
VCCS
VPP
TR
VV
GND
GND
5V
CLK PIN 1

1


5V
STB PIN 2
500µS
VIH
VIL
TPW
VIH
VIL
GND
GND
5V
P/N PIN 2

3


5V
FO PIN 1B
500µS
VCCS
GND
VIH
VIL
GND
5V
FO PIN 2

2

NOTES

1. *Oscilloscope trigger: Pin 2 or 21 of socket adapter 715-1594-2. Trigger on the positive slope. DC coupled.*

2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT

3. *Select calibration step 26 (AND ARRAY), pin 2*
   27 (OR ARRAY), pin 21

4. *Load Vcc with 100 ohm, 1 watt resistor.*

5. *Fill data RAM with hex data FF.*

6. *Pin 19: VIH*
   Pin 22: VIH if AND array
   VIL if OR array

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10	–	50	us	

REVISIONS

ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT.	1/25/82

DATA I/O ISSAQUAH, WA

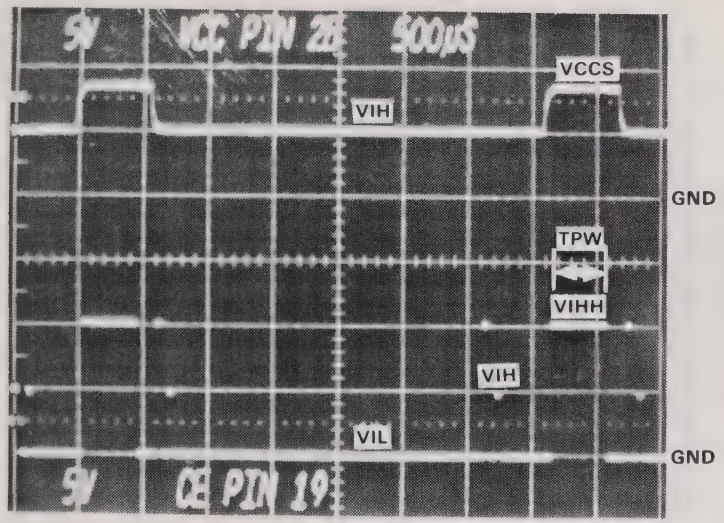
TITLE
TIMING DIAGRAM
SIGNETICS IFL
FPLS AND/OR ARRAY

DRAWN BY:

CHECKED BY: GL

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	34-950-0104

SCALE | SHEET 1/1



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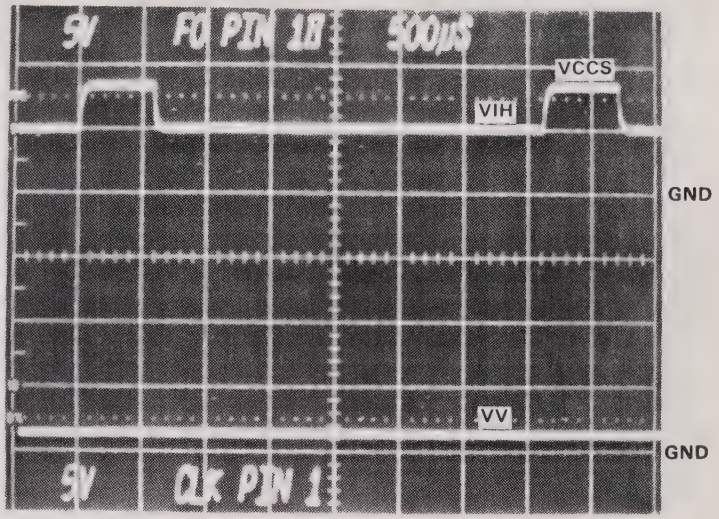


2

NOTES

1. *Oscilloscope trigger: Pin 19 of socket adapter 715-1594-2. Trigger on the positive slope. DC coupled.*
2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT
3. *Select calibration step 28.*
4. *Load Vcc with 100 ohm, 1 watt resistor.*
5. *Fill data RAM with hex data 55.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10	–	50	us	

REVISIONS

ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT.	1/25/82

DATA I/O ISSAQUAH, WA

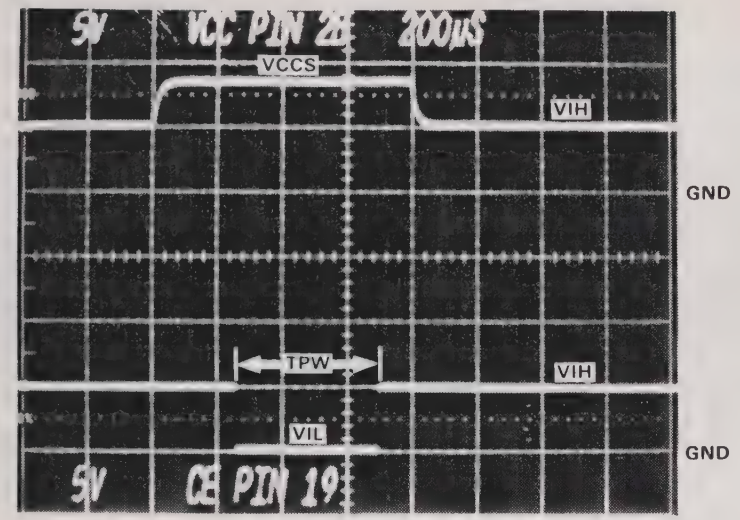
TITLE
TIMING DIAGRAM
SIGNETICS IFL
FPLS PR/OE FUSE

DRAWN BY: KJ

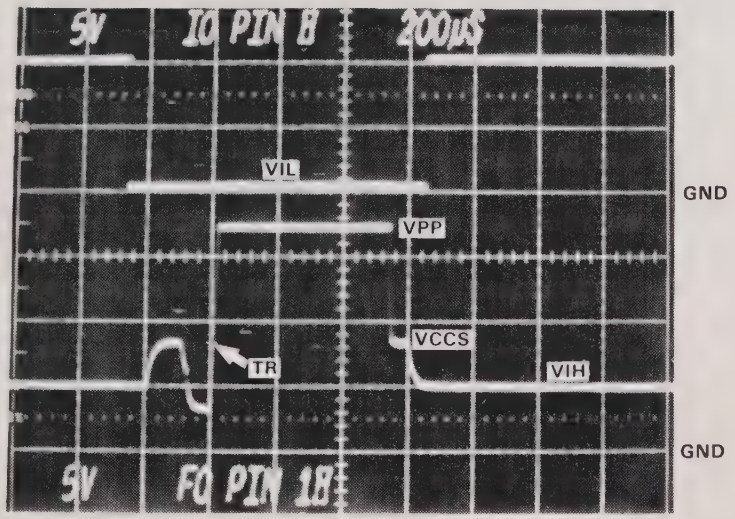
CHECKED BY: GC

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	34-950-0104

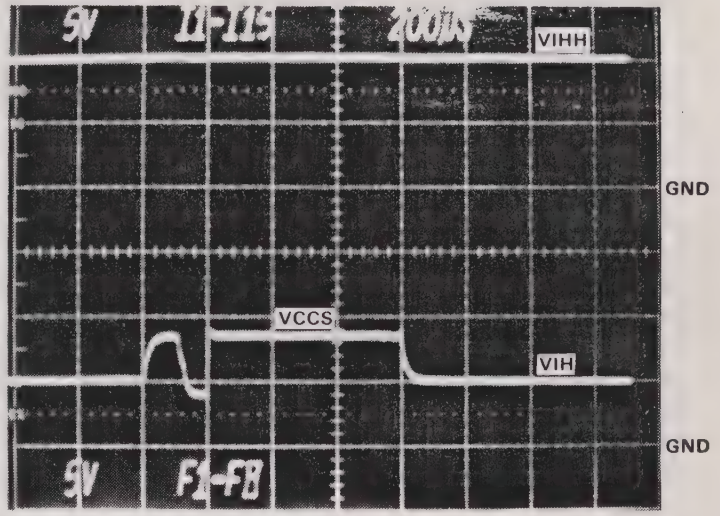
SCALE | SHEET 1/1


5V
VCC PIN 28
200µS
VCCS
VIH
GND
TPW
VIH
VIL
GND
5V
CE PIN 19

1


5V
IO PIN 8
200µS
VIL
GND
VPP
VCCS
TR
VIH
GND
5V
FO PIN 18

2


5V
VIHH
GND
VCCS
VIH
GND
5V
F1-F8

3

NOTES

1. *Oscilloscope trigger: Pin 8 of socket adapter 715-1595. Trigger on the positive slope. DC coupled.*
2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT
3. *Select calibration step 26.*
4. *Load Vcc with 100 ohm, 1 watt resistor.*
5. *Fill data RAM with hex data 55.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10	—	50	us	

REVISIONS

ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT.	1/25/82

DATA I/O ISSAQUAH, WA

TITLE
TIMING DIAGRAM
SIGNETICS IFL
FPGA AND ARRAY

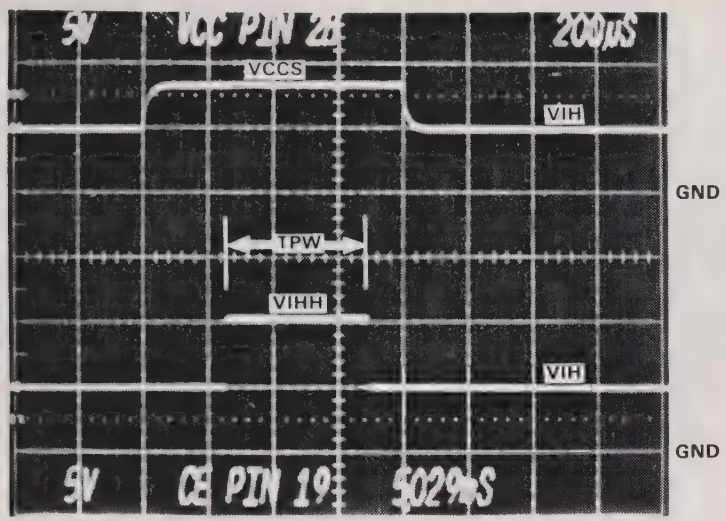
DRAWN BY: KJ

CHECKED BY: GL

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	34-950-0104

SCALE

SHEET 1/1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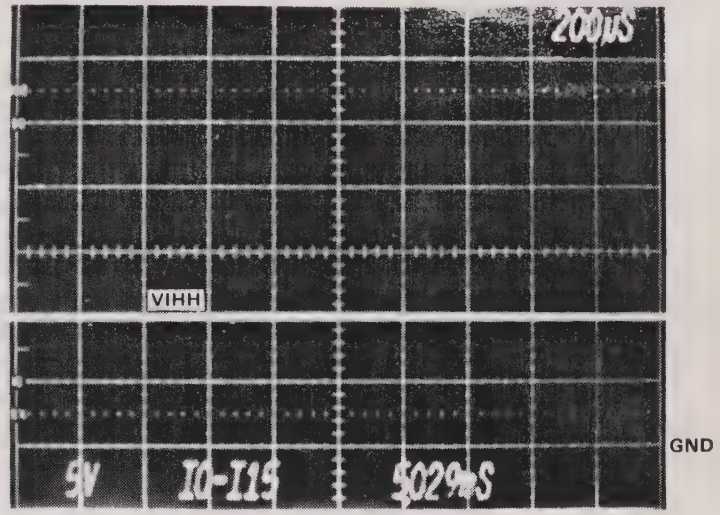
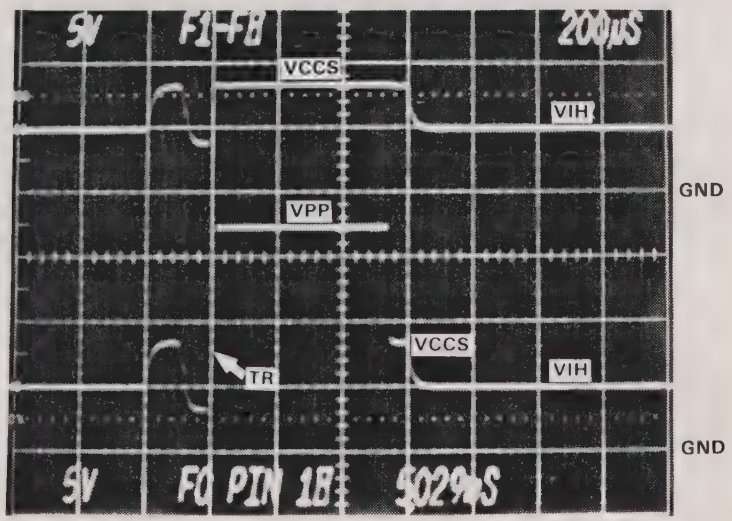
VCC PIN 28
200µS
VCCS
VIH
GND
TPW
VIHH
VIH
GND
5V
CE PIN 19
5029µS

1


200µS
VIHH
GND
5V
IO-I19
5029µS

3


5V
F1-F8
200µS
VCCS
VIH
GND
VPP
VCCS
TR
VIH
GND
5V
FO PIN 18
5029µS

2

NOTES

1. *Oscilloscope trigger: Pin 19 of socket adapter 715-1595. Trigger on the positive slope. DC coupled.*

2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT

3. *Select calibration step 28.*

4. *Load Vcc with 100 ohm, 1 watt resistor.*

5. *Fill data RAM with hex data 55.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10	—	50	us	

REVISIONS

ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT.	1/25/82

DATA I/O ISSAQUAH, WA

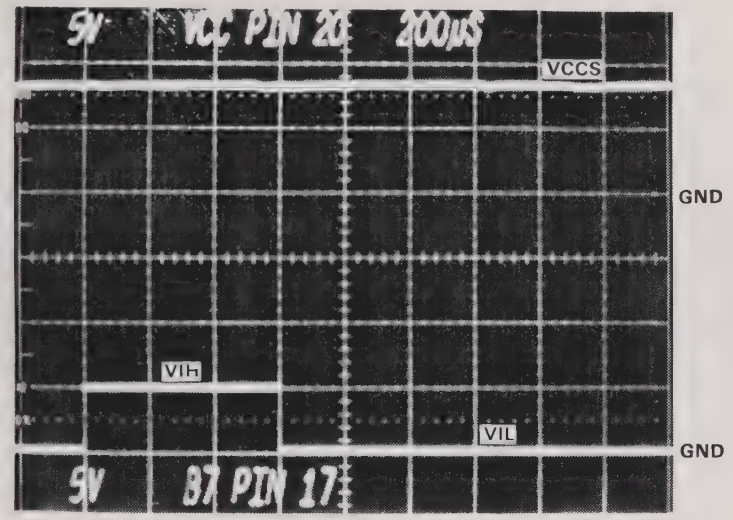
TITLE
TIMING DIAGRAM
SIGNETICS IFL
FPGA OUTPUT POLARITY

DRAWN BY: KJ

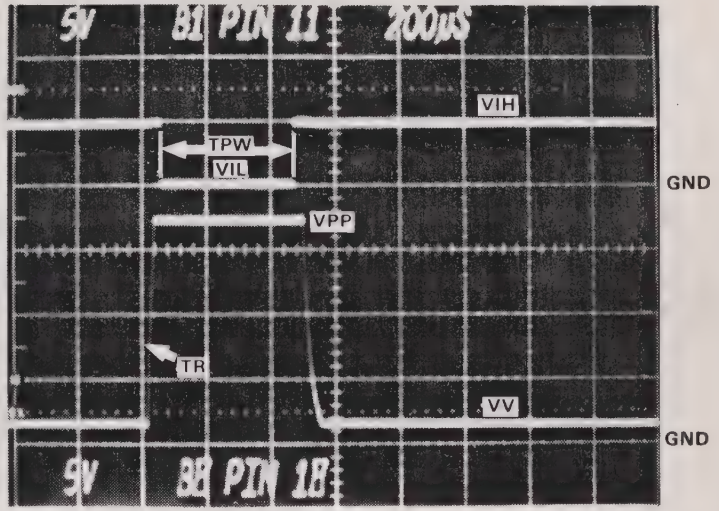
CHECKED BY: GC

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	34-950-0104

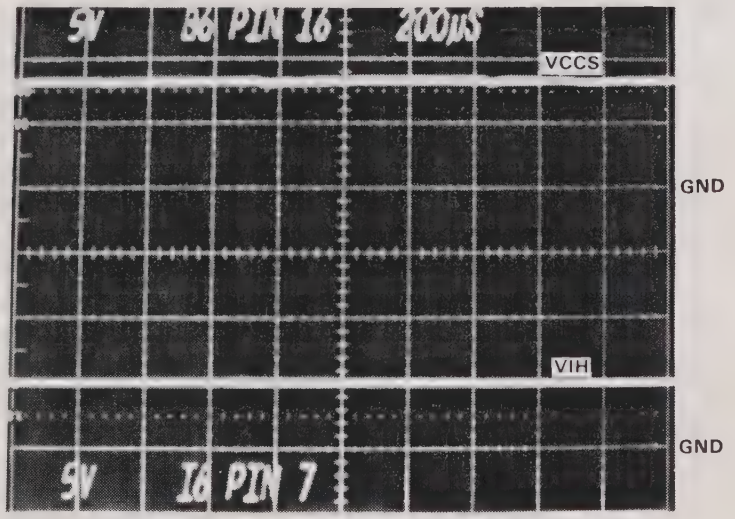
SCALE | SHEET 1/1


5V
VCCS
GND
VIH
VIL
GND
5V

1


5V
VIH
TPW
VIL
GND
VPP
TR
VV
GND
5V

3


5V
VCCS
GND
VIH
GND
5V

2

NOTES

1. *Oscilloscope trigger: Pin 15 of socket adapter 715-0018-001. Trigger on the positive slope. DC coupled.*
2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT
3. *Select calibration step 26 (AND ARRAY)*
   27 (OR ARRAY)
4. *Load Vcc with 100 ohm, 1 watt resistor.*
5. *Fill data RAM with hex data FF.*

WAVEFORM VARIABLES

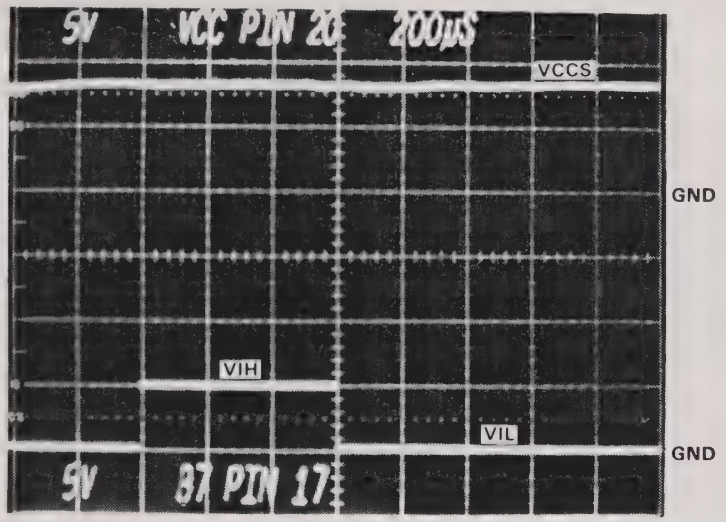
VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10	—	50	us	

REVISIONS

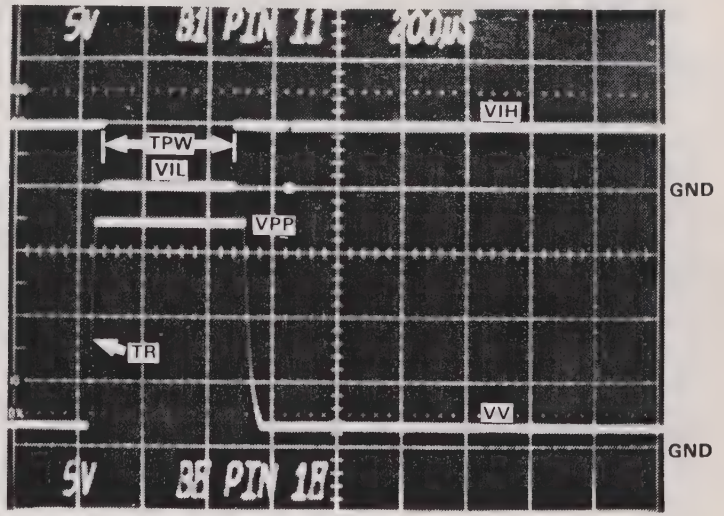
ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT.	1/25/82

DATA I/O ISSAQUAH, WA

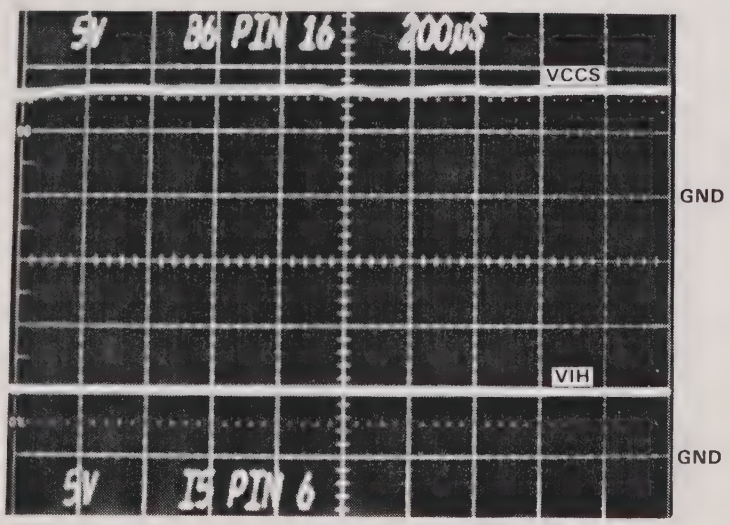
TITLE	TIMING DIAGRAM SIGNETICS IFL 20 PIN FPLA AND/OR ARRAY	DRAWN BY: KJ	
		CHECKED BY: GL	
SIZE: B	CODE IDENT. NO.: 54193	DRAWING NO.: 34-950-0104	
SCALE		SHEET 1/1	


5V
VCC PIN 20
200µS
VCCS
GND
VIH
VIL
GND
5V
87 PIN 17

1


5V
81 PIN 11
200µS
VIH
TPW
VIL
GND
VPP
TR
VV
GND
5V
88 PIN 18

3


5V
86 PIN 16
200µS
VCCS
GND
VIH
GND
5V
19 PIN 6

2

NOTES

1. *Oscilloscope trigger: Pin 6 of socket adapter 715-0018-001. Trigger on the positive slope. DC coupled.*
2. *JP1 = POS A: 1 PULSE REJECT*
   = POS B: 2 PULSE REJECT
3. *Select calibration step 28.*
4. *Load Vcc with 100 ohm, 1 watt resistor.*
5. *Fill data RAM with hex data FF.*

WAVEFORM VARIABLES

VARIABLE	MIN	NOM	MAX	UNIT	COMMENTS
VCCS	8.25	8.50	8.75	V	
VCCP	4.75	5.00	5.25	V	
VIHH	9.50	10.00	10.50	V	
VOP	9.50	10.00	10.50	V	
VPP	16.00	17.00	18.00	V	
VV	1.25	1.50	1.75	V	
VIH	4.75	5.00	5.25	V	
VIL	0.00	0.40	0.80	V	
TPW	300	400	500	us	
TR	10	—	50	us	

REVISIONS

ZONE	LTR	DESCRIPTION		PE.	DATE
	A	RELEASE		WT.	1/25/82

DATA I/O ISSAQUAH, WA

TITLE	**TIMING DIAGRAM SIGNETICS IFL 20 PIN FPLA OUTPUT POLARITY**	DRAWN BY: KJ
		CHECKED BY: GC

SIZE	CODE IDENT. NO.	DRAWING NO.
B	54193	34-950-0104

SCALE | SHEET 1/1

SECTION 5
MAINTENANCE

5.1 CLEANING

Inspect the Logic Pak regularly, inside and out, for accumulated dust and dirt. Dust on the circuit boards is most easily removed with a blast of compressed air. Dust and dirt can be wiped off the outside with a damp cloth. Do not use any abrasive chemical.

5.2 INSPECTION

Periodic inspection of the Logic Pak can be a hedge against malfunction. A good time to schedule an inspection is before a troubleshooting or calibration. Check cable connections, card seating, mounting of discrete components, etc., for shorts, opens, or unstable continuity.

Particular care is required if heat damaged components are found. It is important to find and correct the cause of overheating in order to prevent further damage.

SECTION 6
CIRCUIT DESCRIPTION

6.1 INTRODUCTION

The Logic Pak consists of three cards connected by a cable and housed within the card carrier. These cards provide the interface between the device and the programmer and provide the signals necessary to program and verify devices. Figure 6-1 is the system block diagram. The cards obtain address control, bit information, and raw programming voltages from the programmer's central processing unit (CPU). Software, carried in the PROMs in the programming module, controls the programming algorithm which burns the device fuses, as well as the data entry and RAM formatting routines.

Appendix C contains the schematic diagrams of the programming module's three cards. Each card is described in detail in the following sections and accompanied by a block diagram.

6.2 ANALOG CARD #1

This card houses the output drive circuitry, comparators, data buffers, V_P and $\widehat{VOP}$ generators, V_{CC} generator, V_{FE} switch, overcurrent memory, and backwards-device test circuitry. The following paragraphs explain the operation of the circuits in detail. Figure 6-2 is a block diagram of the card.

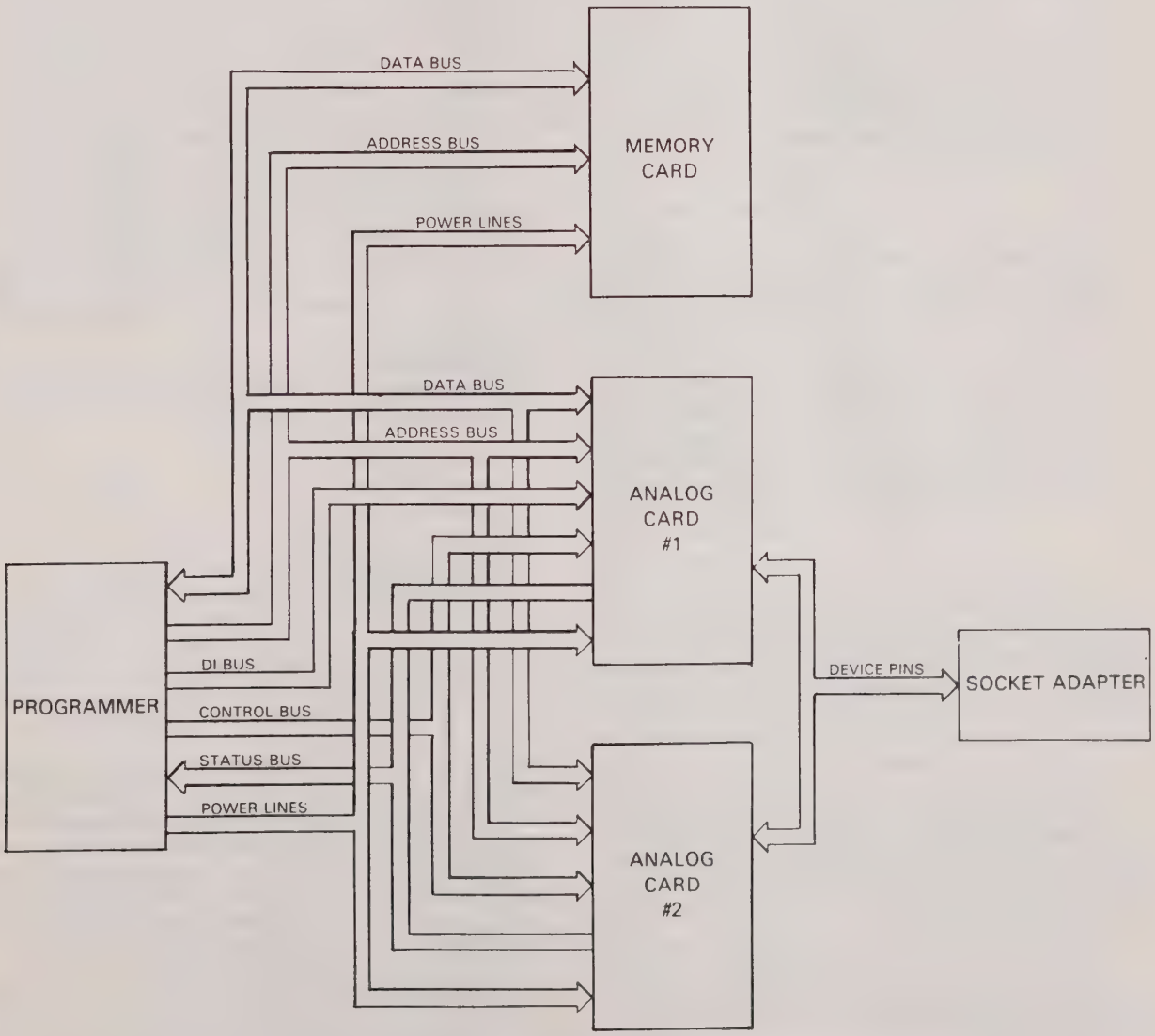


Figure 6-1. System Block Diagram

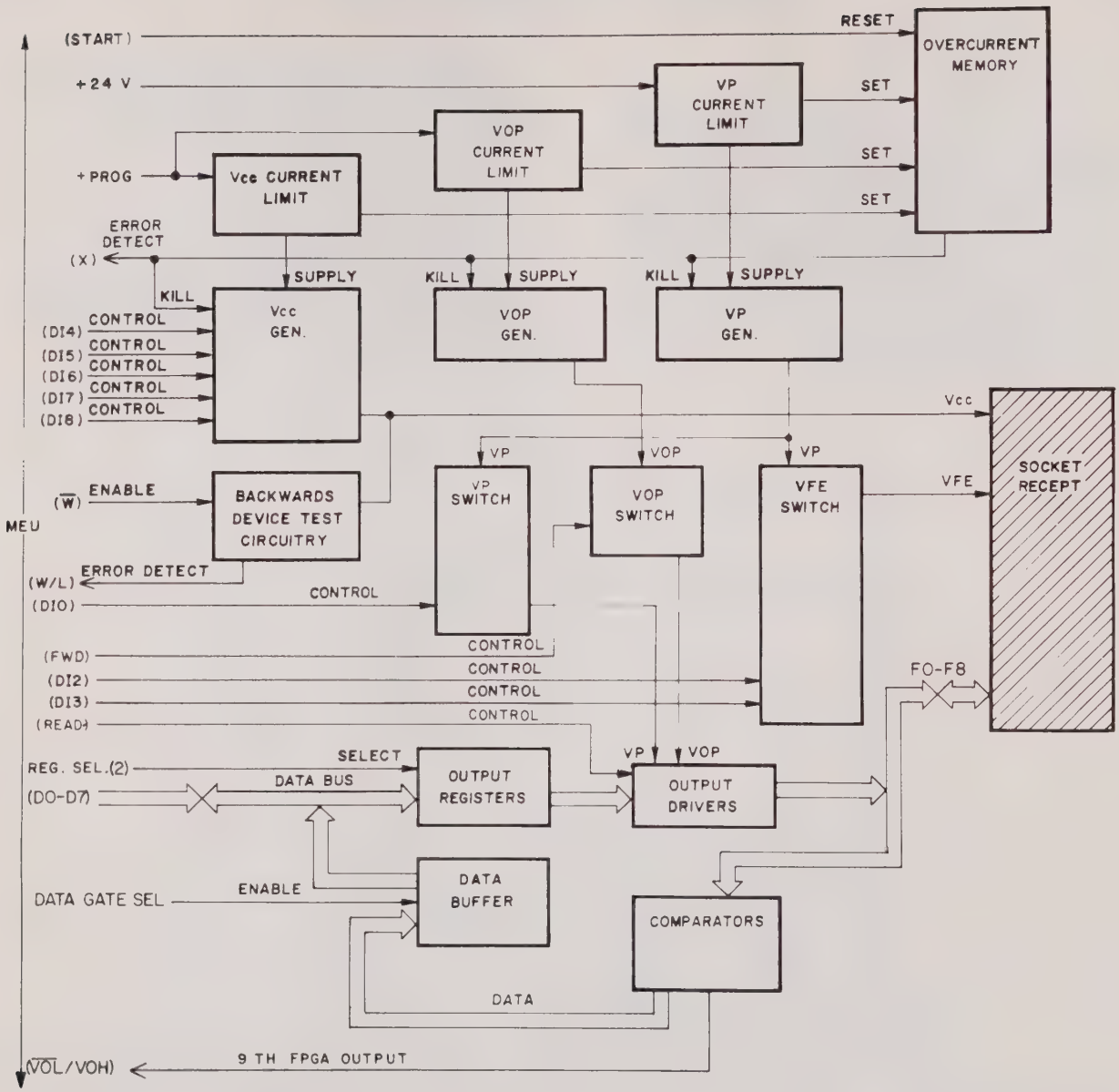


Figure 6-2. Block Diagram, Analog Card #1

6.2.1 OUTPUT REGISTERS

The two octal registers are enabled by the processor via the decode circuitry on Analog Card #2. These registers store two 8-bit bytes of data that control the 16 lines to the output drivers.

6.2.2 OUTPUT DRIVERS

The output drivers are tri-level circuits with two of the three levels obtained by separate current sources and current sink drivers.

The source drivers consist of buffers driving PNP switches. The emitters of the switches are connected to the V_{OP} generator and the V_P switch. When turned on, the PNP switches send the programming voltage to the device. This level is V_{OP} when the V_P switch is off and the V_{OP} switch is on. The level is V_P when the V_P switch is on. The output sinks are eight high current drivers. These provide the TTL Ø level for addressing. The TTL 1 level is obtained by turning both the source and the sink drivers off and letting the pullup resistors set the output level to 5 V.

6.2.3 COMPARATORS AND DATA BUFFER

The comparators provide TTL outputs from a comparison of the device output and a reference level. Outputs are then fed to the data buffer. Enabling the data

buffer allows the programmer to read the states of the device outputs for verification.

6.2.4 V_P GENERATOR

The V_P generator consists of a TL430 shunt regulator (VR1) which controls a Darlington pass transistor (Q3). Feedback is provided to the TL430 by a voltage-adjusting potentiometer (R3). Current limiting occurs when the current through R3 creates enough voltage drop to turn on Q1. The output of Q1 sets the overcurrent memory.

6.2.5 V_{OP} GENERATOR

This supply is of the same design as the V_P generator. The only differences are in the output voltage (set by R29) and the current limit threshold. Current limiting happens when Q19 is turned on by the voltage drop across R33.

6.2.6 V_{CC} GENERATOR

The 5-level V_{CC} generator consists of an IC regulator (U1) driving a pass transistor (Q5). Four of the five V_{CC} levels are preset by potentiometers (R51-R54). The fifth V_{CC} output level is 0 V (V_{CC} Kill) with no adjustment. Current limiting occurs when the emitter-base junction of Q18 is forward-biased by the voltage drop across R26. The output of Q18 sets the overcurrent memory. The V_{CC} generator's output voltage rise time is set by the value of C7.

6.2.7 V_P SWITCH

This switch, when on, sends the V_P level to the output drivers. The switch consists of two PNP transistors (Q16 and Q17). The rise time is set by the RC value of R34 and C6.

6.2.8 V_{FE} SWITCH

This switch provides two voltages to the Program pin of the IFL device. The two levels are V_P and V_V. Active pullup circuitry, consisting of transistors Q14 and Q15, provides the V_P level. The RC value of R8 and C5 sets the V_P rise time. When the pullup circuit is off, the clamping network of CR2, CR3, and R4 clamps the switch output to the V_V level. During an overcurrent condition, the pullup circuit is held off by the overcurrent memory.

6.2.9 V_{OP} SWITCH

This switch sends the level of the V_{OP} generator to the emitters of the output switches. The circuitry is identical to the V_P switch described above.

6.2.10 OVERCURRENT MEMORY

When a current limit condition is detected by any one of the generators, base current is applied to Q22 of the overcurrent memory. This transistor is the NPN of an SCR memory. Turning on the NPN applies base drive to the PNP; the PNP turns on, providing drive for the NPN. This stable state remains until the NPN is turned off via the Start line from the control register. Output from this memory is used to shut down the power supplies and to signal the processor that an overcurrent condition exists.

6.2.11 BACKWARDS-DEVICE TEST CIRCUITRY

A comparator and a saturated switch are used for the backwards-device tests. The comparator input and switch output are tied to the V_{CC} pin of the device. The switch is turned on, connecting the V_{CC} pin to 5 V through a resistor. If the device is inserted backwards, the voltage drop across R62 creates a voltage less than the comparator reference. The comparator outputs a TTL Ø, which is detected to flag an error. Further operation is prevented, protecting the device.

During this test, all input and output device pins are held at the TTL 1 level and the V_{CC} generator is held off.

6.3 ANALOG CARD #2

This card houses the device input-drive circuitry, the input-drive voltage generator (V_{IHH}), PROM and RAM memory, and the decode circuitry. Figure 6-3 is a block diagram of this card.

6.3.1 INPUT REGISTERS

These four octal registers are enabled by the decode circuitry. The registers store four, 8-bit bytes of data that control the 32 lines to the input drivers.

6.3.2 INPUT DRIVERS

The input drivers consist of four 75367 quad MOS drivers. These circuits output the V_{IHH} generator and TTL Ø levels. A third level, TTL 1, is accomplished by allowing the pullup resistors to set the levels to 5 V when the drivers are disabled.

6.3.3 V_{IHH} GENERATOR

The V_{IHH} generator consists of a TL430 shunt regulator driving a Darlington pass transistor. Feedback is provided to the TL430 by the voltage-adjusting potentiometer (R4). In the case of an overcurrent condition, Q3 turns on, setting the overcurrent memory. The overcurrent memory holds the base of the pass transistor low.

6.3.4 DECODE CIRCUITRY

The decode circuitry consists of two PROMs, one 256 x 4 (U17) and one 32 x 8 (U18). These monitor the address bus, providing enables to the registors, data gates, and memory devices that connect to the data bus. The PROM outputs are clocked with $\overline{V \bullet Ø2}$ so that these devices are active only during that time.

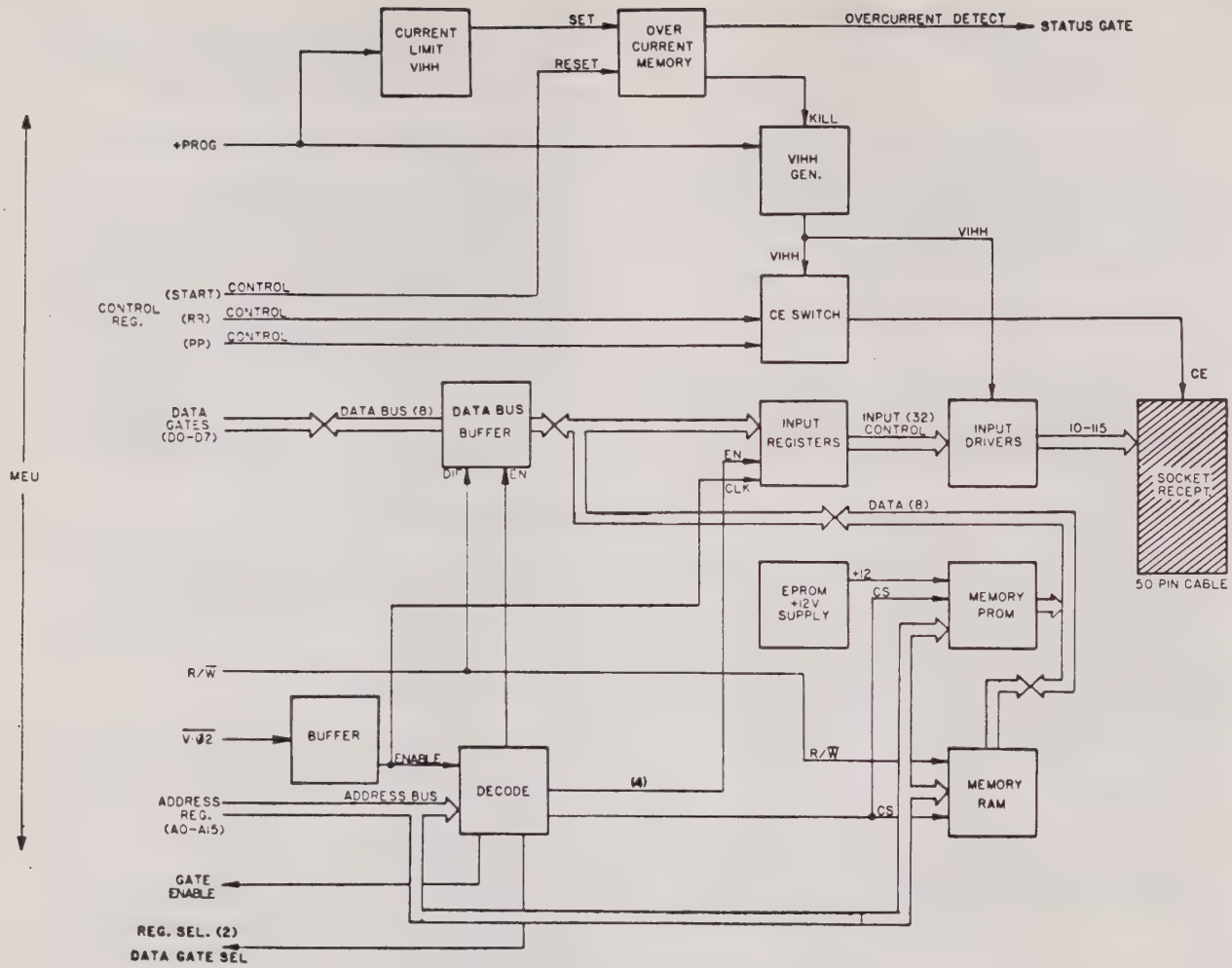


Figure 6-3. Block Diagram, Analog Card #2

6.3.5 PROM AND RAM MEMORY

Two 2716 EPROMs store the programming software. This software controls all Verify, Program, and calibration operations. A 128 x 8 RAM provides scratch-pad storage for software operations.

6.3.6 DATA BUS BUFFER

Data from RAM and PROM is sent to the bidirectional data bus buffer. The buffer sends and receives data from the data bus and outputs to the input registors from the data bus.

6.3.7 $\overline{CE}$ DRIVER

The $\overline{CE}$ driver is identical to the input drivers previously described, providing three levels to the $\overline{CE}$ and PR/$\overline{OE}$ pins of the devices.

6.3.8 OVERCURRENT-DETECT CIRCUITY AND OVERCURRENT MEMORY

The VIHH generator uses foldback current limiting. When the current limit is reached, the overcurrent memory is set, shutting down the supply. (See paragraph 6.2.10.) Current limit is detected when Q3 is biased by the voltage drop across R6.

6.4 MEMORY CARD

The Memory Card is shown in block diagram form in Figure 6-4. PROMs which store logic entry software are contained on the Memory Card. These PROMs connect to the address bus directly and to the data bus through data buffers. Monolithic regulator Q1 is the 12 V source for the 2716 PROMs.

Two PROMs and a latch comprise the primary decoder. The PROMs connect to 12 higher-order address lines and the R/W line. A 1-of-8 decoder, timed with V•Ø2, provides the secondary decoding for the software PROMs.

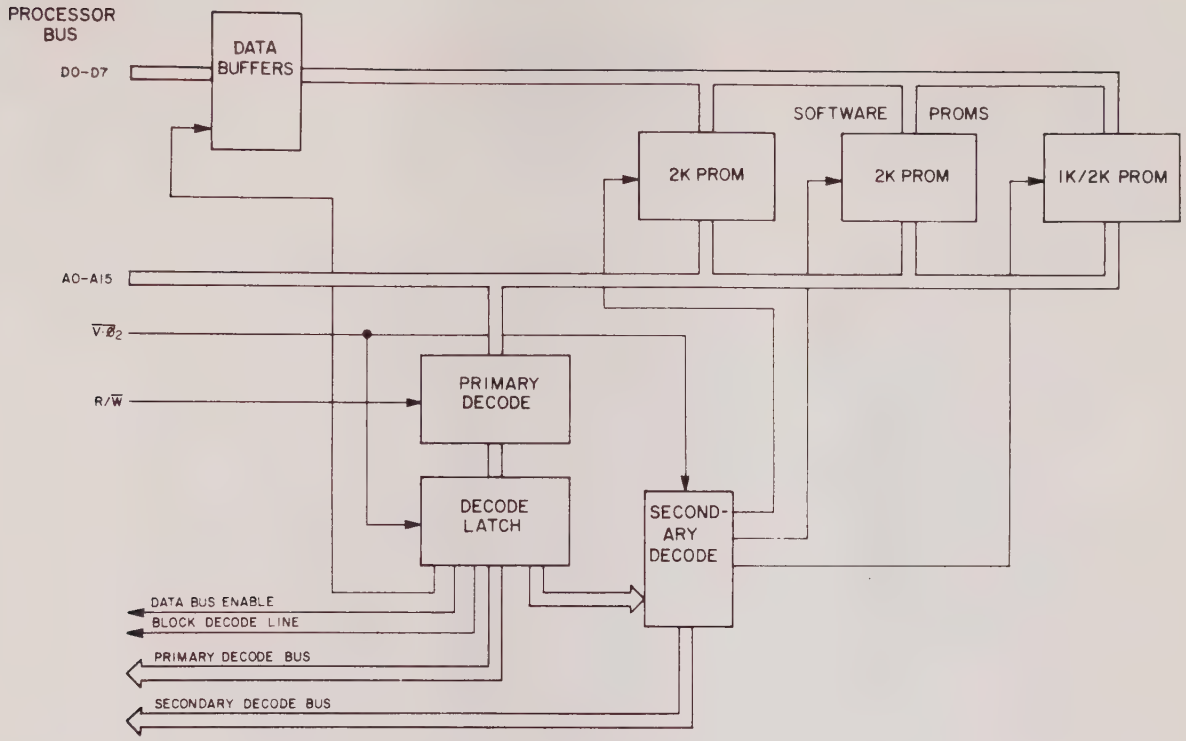
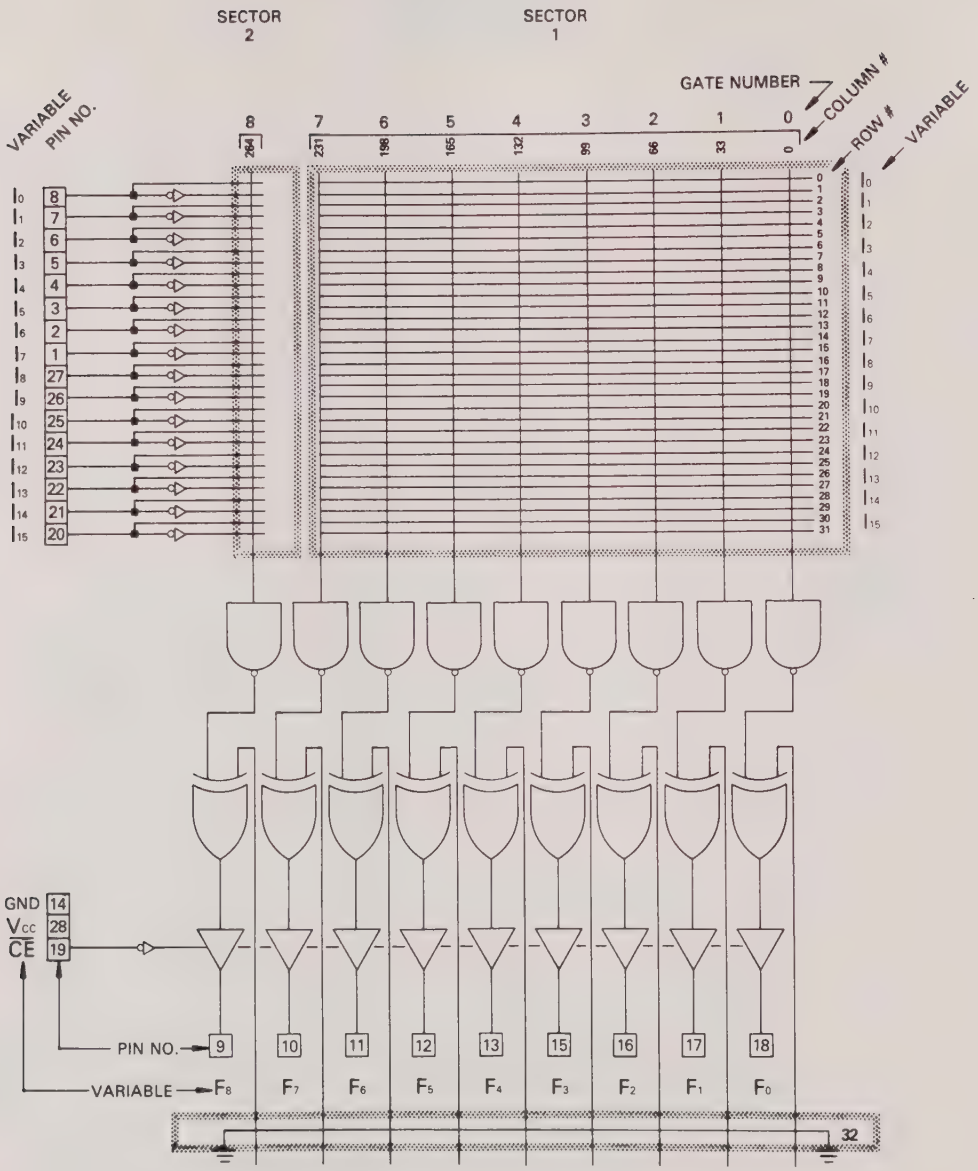


Figure 6-4. Block Diagram, Memory Card

APPENDIX A
LOGIC DIAGRAMS

A-1 Series 28 FPGA
A-2 Series 28 FPLA
A-3 Series 28 FPRP
A-4 Series 28 FPLS
A-5 Series 20 FPLA

SERIES 28 FPGA
LOGIC DIAGRAM


SECTOR 2
SECTOR 1
GATE NUMBER
COLUMN #
ROW #
VARIABLE
VARIABLE PIN NO.
8 7 6 5 4 3 2 1 0
264 231 198 165 132 99 66 33 0
GND 14
Vcc 28
CE 19
PIN NO. 9 10 11 12 13 15 16 17 18
VARIABLE F8 F7 F6 F5 F4 F3 F2 F1 F0
32

NOTE
Grey boxes enclose programmable fuses

Column # + Row # = Fuse #
Example: 33 + 11 = 44

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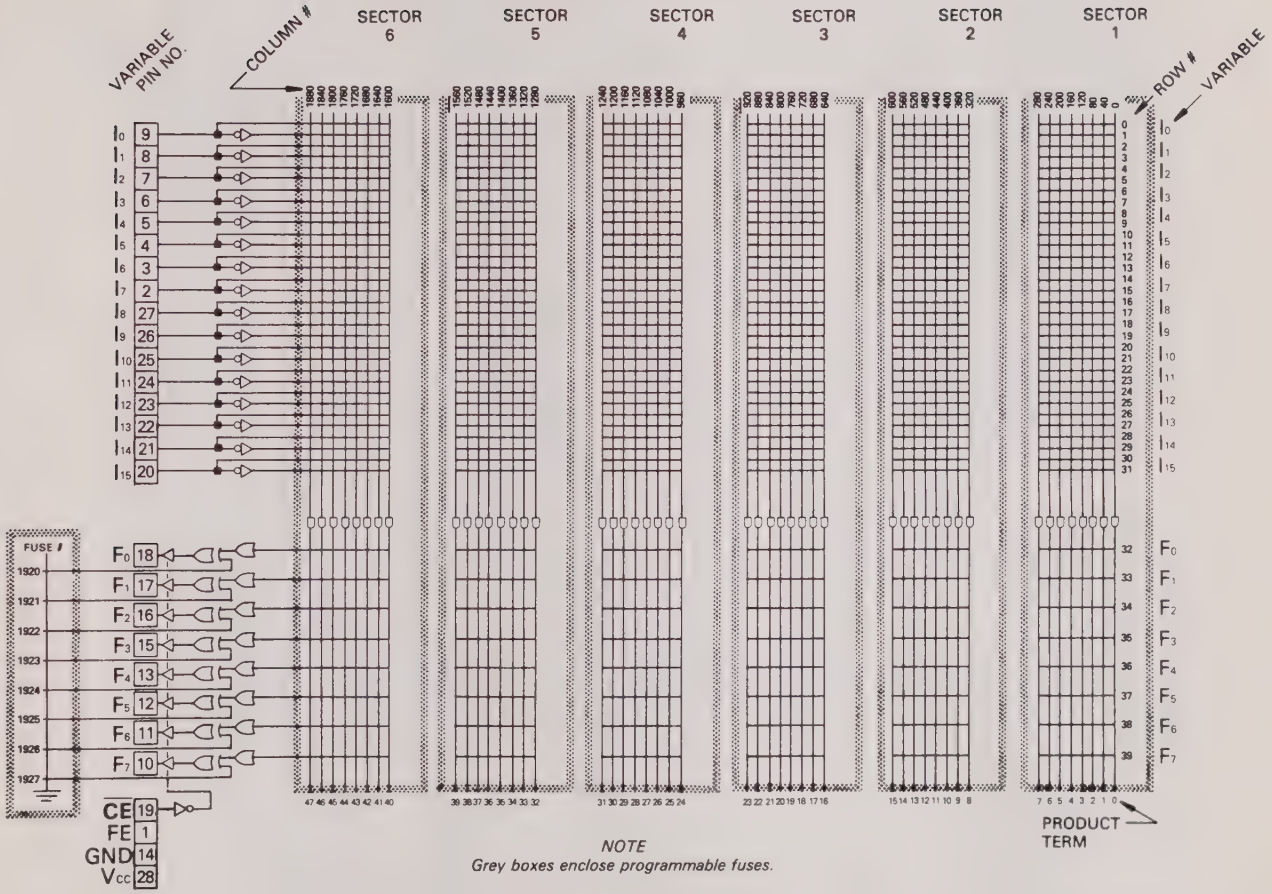
Figure A-1

SERIES 28 FPLA
LOGIC DIAGRAM



NOTE
Grey boxes enclose programmable fuses.

Column # + Row # = Fuse #
Example: 240 + 5 = 245

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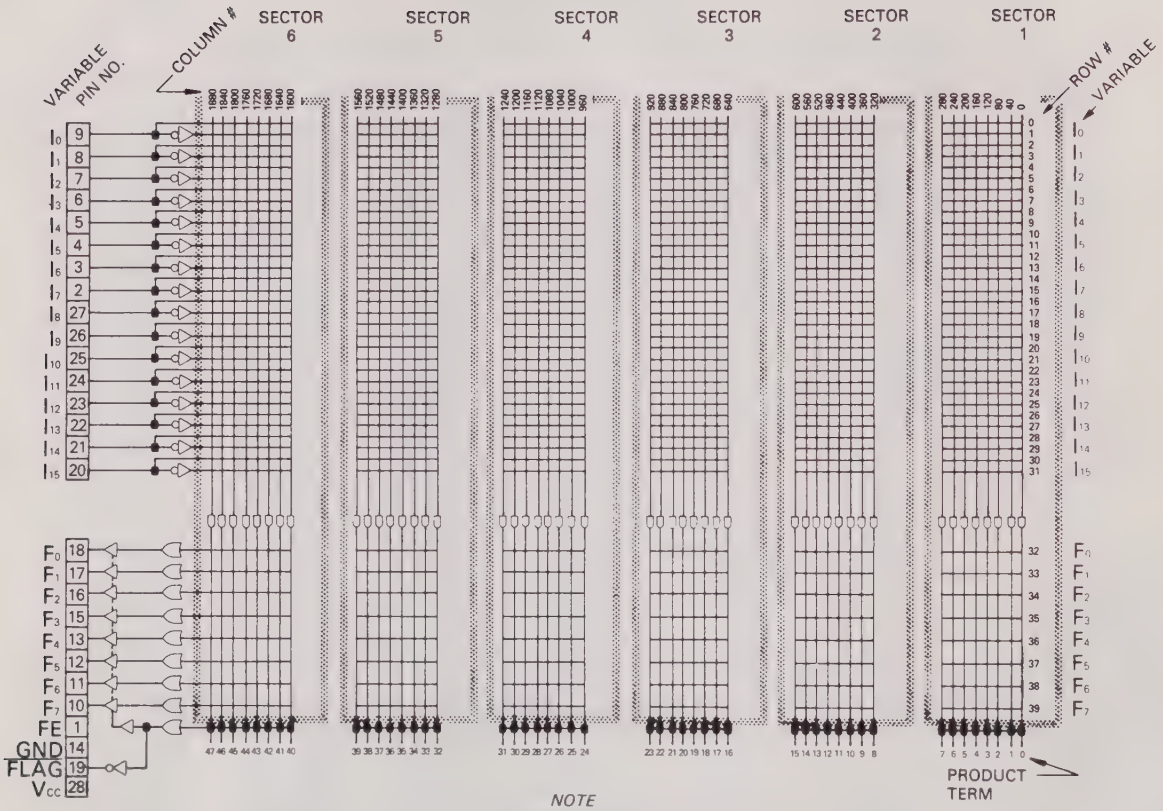
Figure A-2

SERIES 28 FPRP
LOGIC DIAGRAM



NOTE
Grey boxes enclose programmable fuses.

Column # + Row # = Fuse #
Example: 80 + 2 = 82

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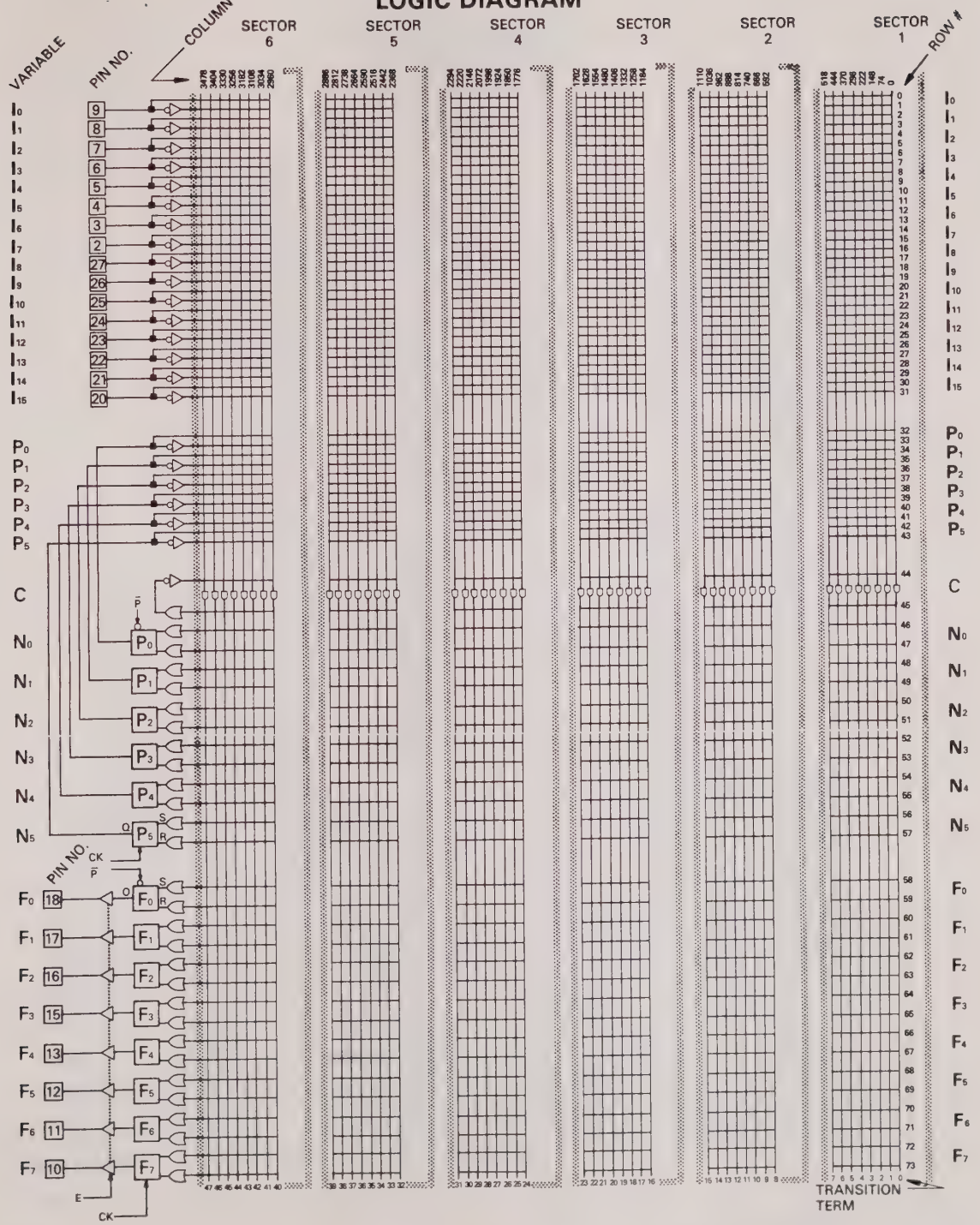
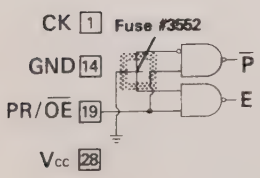
Figure A-3

SERIES 28 FPLS
LOGIC DIAGRAM





NOTE
Grey boxes enclose programmable fuses.

Column # + Row # = Fuse #
Example: 518 + 4 = 522

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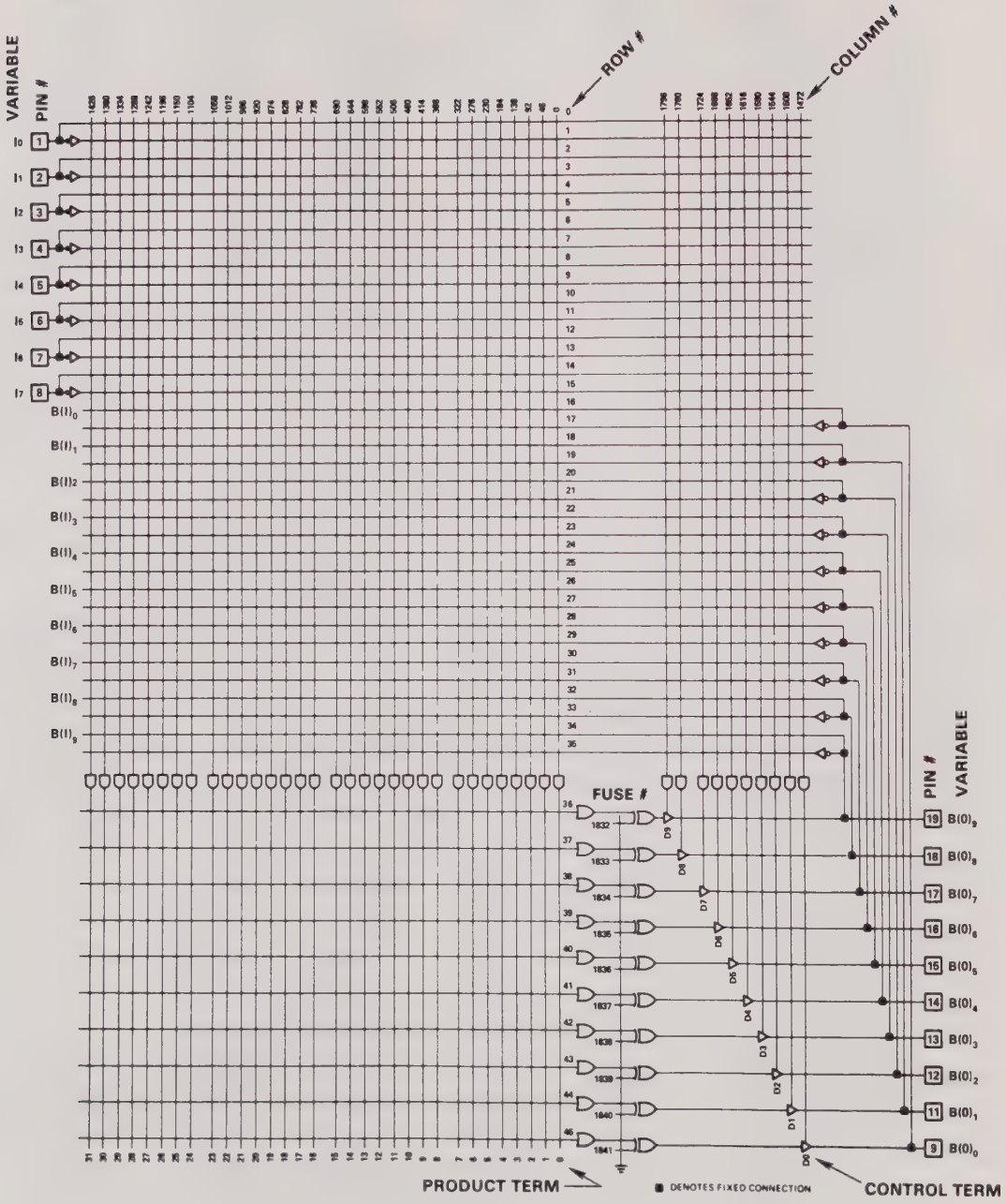
Figure A-4

SERIES 20 FPLA
LOGIC DIAGRAM



Column # + Row # = Fuse #

Example: 46 + 3 = 49

Figure A-5

APPENDIX B
REFERENCE MATERIAL

Table B-1. Glossary
Table B-2. Abbreviations
Table B-3. Cross-Reference Chart of Number Bases
Table B-4. ASCII and IEEE Code Chart
Table B-5. ASCII Control Characters

Table B-1. Glossary

address field. Optional set of control characters in a data translation format. It defines the address of the next data byte.

address offset. A 4-digit hex value subtracted from addresses on input and then added to addresses output from the programmer. The result is added to the begin device address or begin RAM address as applicable.

begin device address. The first device address from which or to which data is being transferred.

begin RAM address. The first address of the programmer data RAM from which or to which data is to be transferred.

blank check. A test performed by a programmer to detect the presence of any programmed bits. A device with no programmed bits is "blank."

block size. The hexadecimal number of bytes to be transferred in a data transfer.

bootstrap. The basic software routine which performs initial power-up machine checks and prepares the machine to receive and respond to operating system instructions.

configuration number. A 4-digit hex number that identifies the software revision level of the programmer.

data translation format. Form in which the translator software accepts input data. Also the form for data output by the unit.

default value. The value the unit uses for a parameter unless the operator specifies another value.

device. Any PROM, EPROM, MOS PROM, or programmable logic array.

end code. Character in a data translation format which signals the completion of a data transfer.

error code. A code which signals specific errors to the operator.

Family and Pinout Codes. Two-digit codes used by some Data I/O programming modules to identify programming variables including pinout, address limit, and programming algorithms.

full duplex. Simultaneous two-way independent transmission in both directions.

generic family. Devices of different memory size developed by a manufacturer that require the same programming voltages, currents, and timing relationships. They can be programmed by the same programming module.

handshaking. The required sequence of signals for communication between two units. The I/O bus protocol for a unit defines its handshaking requirements. This is especially true for asynchronous I/O systems in which each signal requires a response to complete an I/O operation.

half duplex. Transmission alternately in either direction but not both directions simultaneously.

illegal-bit test. A test performed by a programmer to detect the presence of any programmed bits of incorrect polarity (illegal bits).

logic gate. Digital circuits with two or more logic inputs and one output, with a logic level determined by the logic levels present at the inputs. The basic logic gates are:

OR produces a 1 (hi) when one or more inputs are 1.
AND produces a 1 only when all inputs are 1.
NOR produces a Ø (low) when any input is 1.
NAND produces a Ø only when all inputs are 1.
EX-OR produces a 1 only when the two inputs are at different levels.
EX-NOR produces a 1 only when the inputs are at the same logic level.

mode. A software routine in a machine, characterized by a specific automatic sequence of steps.

nibble. One half of an 8-bit byte.

programming module. Generic term for Data I/O Programming Pak, Program Card Set, UniPak, Gang Module, FPLF Pak, MOS Pak, IFL Pak, and other programming electronics.

record size. The number of bytes printed on a line of a teletype or other printer; or the number of bytes printed on a paper tape before another address field is printed.

scratch pad memory. The internal memory used for performing calculations.

Select Function. (Also Select Code) A 2-digit hex number used to specify data translation formats, serial interface operations, or certain RAM data manipulations.

start code. Character in a data translation format which signals the beginning of a data transfer.

sum-check. A summation of bits calculated according to the rules of simple addition and usually expressed as a

4-digit hex number; any carry from the most significant bit or digit is discarded. A sum-check is used to verify the integrity of data transfers.

HEX DATA	BINARY DATA
84	10000100
C1	11000001
62	01100010
24	00100100
01CB	0000 0001 1100 1011
↑ Sum-check in hexadecimal notation	↑ Sixteen-bit binary sum-check

Figure B-1. Sample Sum-check Calculation

truth table. (Also function table.) A table used to analyze logic gates by showing all the input and output possibilities.

waveforms (programmable). The graphical representation of the timing and magnitude of programming pulses. If the programming waveforms are not kept within tolerance, programming yield is jeopardized.

word limit. The highest address in a device. For example, the word limit of a 1Kx8 device is 1K (or hex 3FF). Synonymous with address limit.

word width. The number of bits in a byte or word (4 or 8).

Table B-2. Abbreviations

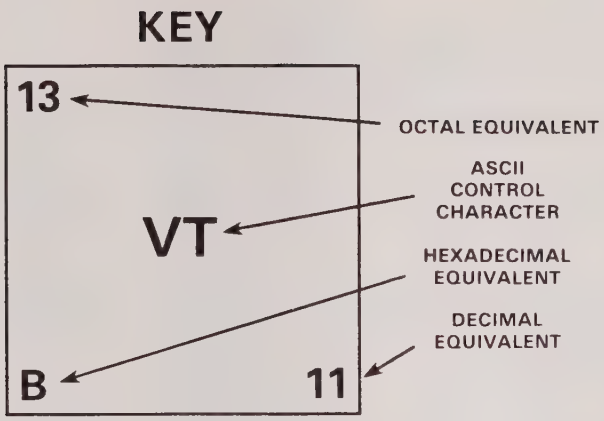
The following is a list of abbreviations commonly used in Data I/O Instruction manuals.

A_4 - address line 4
ADDR - address
BC - bin count, number of bins
BR - bridge rectifier
C - capacitor
$\overline{CE}$ - Chip Enable
Clk - clock
Clk. Inh. - clock inhibit
Cntl. - control
Cont. - control
CR - diode
CTS - Clear To Send
D_5 - data line 5
DAC - Digital to Analog Converter
DC - division count, number of partitions
DCD - Data Carrier Detect
DCU - Data I/O Data Control Unit
DI_2 - data input 2
DIR - Directory
DO_2 - data output 2
DS - display
DSR - Data Set Ready
DTR - Data Terminal Ready
DVM - digital voltmeter
Emul - emulate
ERR - error
ESC - escape
F - fuse
FC - Translation Format Code
FFPP - Family Code (FF) and Pinout Code (PP)
FIP - Flourescent Indicator Panel
FPGA - Field Programmable Gate Array
FPLA - Field Programmable Logic Array
FPLS - Field Programmable Logic Sequencer
FPRP - Field Programmable ROM Patch
FRME - frame
Fwd. - Forward
Gnd. - Ground
HLT. - Halt
HV - high voltage
ID_4 - identification line 4
IFL - Integrated Fused Logic
I/O - Input/Output
$\overline{IRQ}$ - Interrupt Request
J - jack or connector
JP - jumper
K - relay
LIM - limit
LSB - Least Significant Bit
LSD - Least Significant Digit
MSB - Most Significant Bit
MSD - Most Significant Digit
NMI - Non-Maskable Interrupt
NO CONT SECT - No Contiguous Sector
Oper. - operate
PA_{15} - programmer address line 15
PAK - programming module
PCS - Program Card Set
PD_6 - programmer data line 6
PN - Part Number
PR/$\overline{OE}$ - Preset/Output Enable
Prog - Program
Prog. Pulse - Program Pulse
PROM - Programmable Read Only Memory
Q - transistor
R - resistor
RAM - Random Access Memory
Read Inh. - Read Inhibit
Rec. - receive
Rev. - reverse
RP - resistor pack
RST - Reset
R/$\overline{W}$ - Read/Write
RX - Receive Data
S - switch
TOR - Turn On Reset
TX - Transmit Data
U - integrated circuit device
$\overline{V \bullet \emptyset 2}$ - the "AND"-ing of the Valid Memory Address line and the phase 2 line
Ver. A - Verify pass A
Ver. B - Verify pass B
VFY - verify
VMA - Valid Memory Address
VR - Voltage Regulator
V_{REF} - Voltage Reference
W/L - Word Limit
Write Inh. - Write Inhibit

Table B-3. Cross-Reference Chart of Number Bases

Binary	Octal	Hexadecimal	Decimal	Standard Abbreviation
0000	0	0	0	
0001	1	1	1	
0010	2	2	2	
0011	3	3	3	
0100	4	4	4	
0101	5	5	5	
0110	6	6	6	
0111	7	7	7	
1000	10	8	8	
1001	11	9	9	
1010	12	A	10	
1011	13	B	11	
1100	14	C	12	
1101	15	D	13	
1110	16	E	14	
1111	17	F	15	
0001 0000	20	10	16	
0010 0000	40	20	32	
0100 0000	100	40	64	
1000 0000	200	80	128	
0001 0000 0000	400	100	256	
0010 0000 0000	1000	200	512	
0100 0000 0000	2000	400	1,024	1K
1000 0000 0000	4000	800	2,048	2K
1100 0000 0000	6000	C00	3,072	3K
0001 0000 0000 0000	10000	1000	4,096	4K
0001 0100 0000 0000	12000	1400	5,120	5K
0001 1000 0000 0000	14000	1800	6,144	6K
0001 1100 0000 0000	16000	1C00	7,168	7K
0010 0000 0000 0000	20000	2000	8,192	8K
0010 0100 0000 0000	22000	2400	9,216	9K
0010 1000 0000 0000	24000	2800	10,240	10K
0100 0000 0000 0000	40000	4000	16,384	16K
1000 0000 0000 0000	100000	8000	32,768	32K
0001 0000 0000 0000 0000	200000	10000	65,536	64K

Table B-4. ASCII & IEEE Code Chart



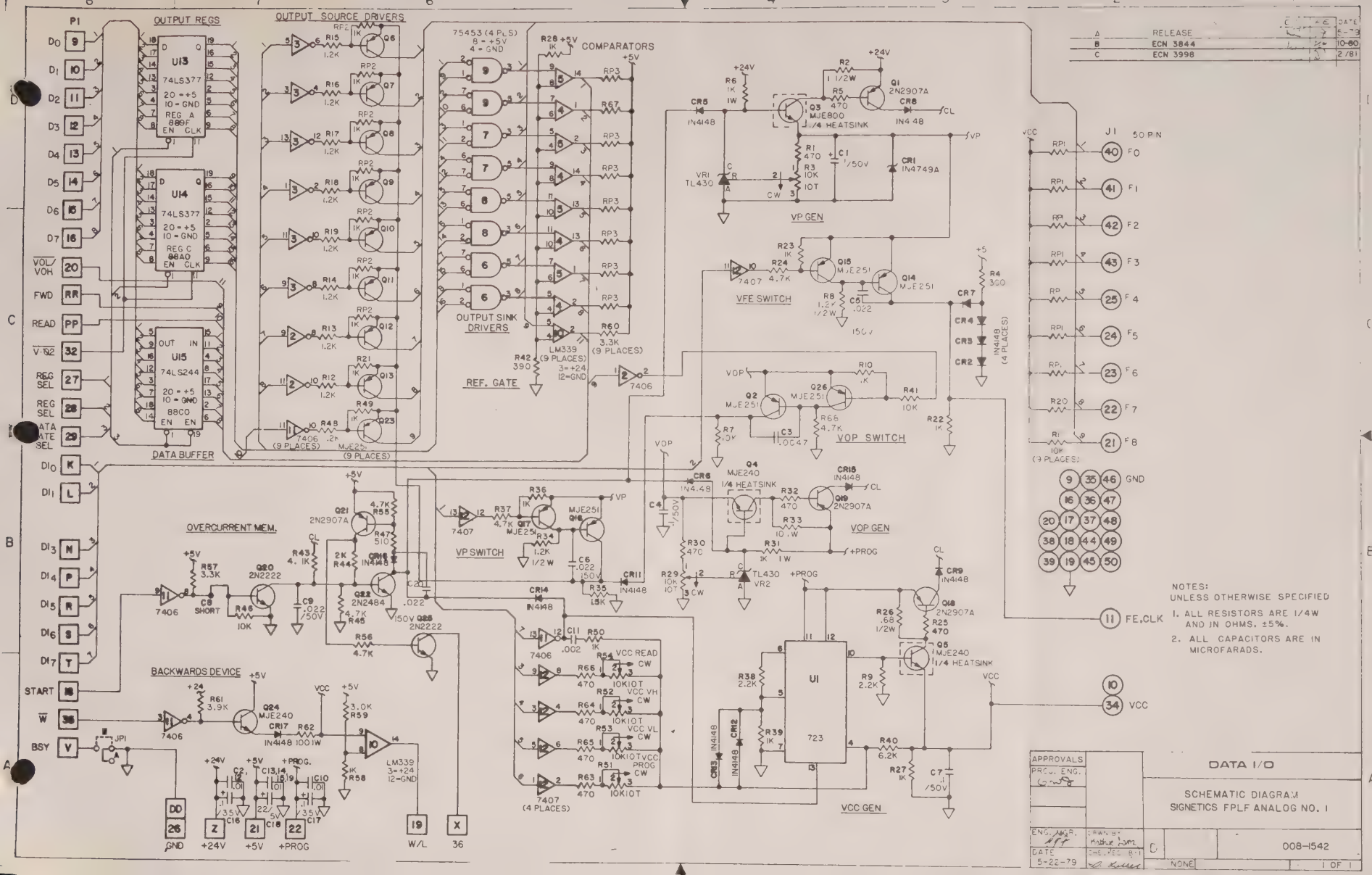
7 6 5 / BITS 4 3 2 1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS & SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0 0	20 DLE 10 16	40 SP 20 32	60 0 30 48	100 @ 40 64	120 P 50 80	140 ` 60 96	160 p 70 112
0 0 0 1	1 SOH 1 1	21 DC1 11 17	41 ! 21 33	61 1 31 49	101 A 41 65	121 Q 51 81	141 a 61 97	161 q 71 113
0 0 1 0	2 STX 2 2	22 DC2 12 18	42 " 22 34	62 2 32 50	102 B 42 66	122 R 52 82	142 b 62 98	162 r 72 114
0 0 1 1	3 ETX 3 3	23 DC3 13 19	43 # 23 35	63 3 33 51	103 C 43 67	123 S 53 83	143 c 63 99	163 s 73 115
0 1 0 0	4 EOT 4 4	24 DC4 14 20	44 $ 24 36	64 4 34 52	104 D 44 68	124 T 54 84	144 d 64 100	164 t 74 116
0 1 0 1	5 ENQ 5 5	25 NAK 15 21	45 % 25 37	65 5 35 53	105 E 45 69	125 U 55 85	145 e 65 101	165 u 75 117
0 1 1 0	6 ACK 6 6	26 SYN 16 22	46 & 26 38	66 6 36 54	106 F 46 70	126 V 56 86	146 f 66 102	166 v 76 118
0 1 1 1	7 BEL 7 7	27 ETB 17 23	47 ' 27 39	67 7 37 55	107 G 47 71	127 W 57 87	147 g 67 103	167 w 77 119
1 0 0 0	10 BS 8 8	30 CAN 18 24	50 (28 40	70 8 38 56	110 H 48 72	130 X 58 88	150 h 68 104	170 x 78 120
1 0 0 1	11 HT 9 9	31 EM 19 25	51) 29 41	71 9 39 57	111 I 49 73	131 Y 59 89	151 i 69 105	171 y 79 121
1 0 1 0	12 LF A 10	32 SUB 1A 26	52 * 2A 42	72 : 3A 58	112 J 4A 74	132 Z 5A 90	152 j 6A 106	172 z 7A 122
1 0 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	73 ; 3B 59	113 K 4B 75	133 [5B 91	153 k 6B 107	173 { 7B 123
1 1 0 0	14 FF C 12	34 FS 1C 28	54 , 2C 44	74 V 3C 60	114 L 4C 76	134 \ 5C 92	154 l 6C 108	174 | 7C 124
1 1 0 1	15 CR D 13	35 GS 1D 29	55 - 2D 45	75 = 3D 61	115 M 4D 77	135] 5D 93	155 m 6D 109	175 } 7D 125
1 1 1 0	16 SO E 14	36 RS 1E 30	56 . 2E 46	76 > 3E 62	116 N 4E 78	136 ^ 5E 94	156 n 6E 110	176 ~ 7E 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 2F 47	77 ? 3F 63	117 O 4F 79	137 — 5F 95	157 o 6F 111	177 Rubout 7F 127
	Addressed Commands	Universal Commands	Listen Addresses		Talk Addresses		Secondary Addresses or Commands	

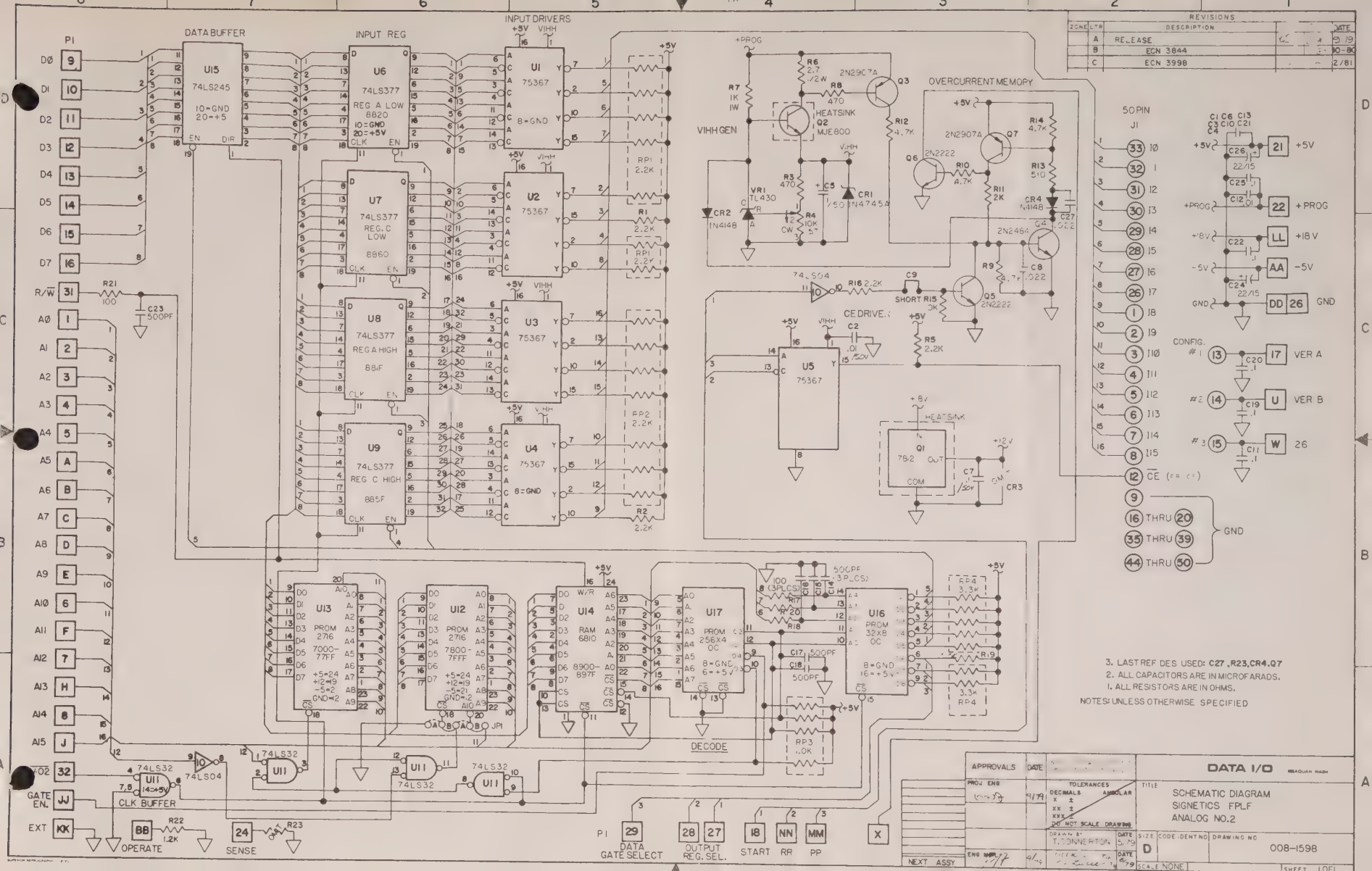
Table B-5. ASCII CONTROL CHARACTERS

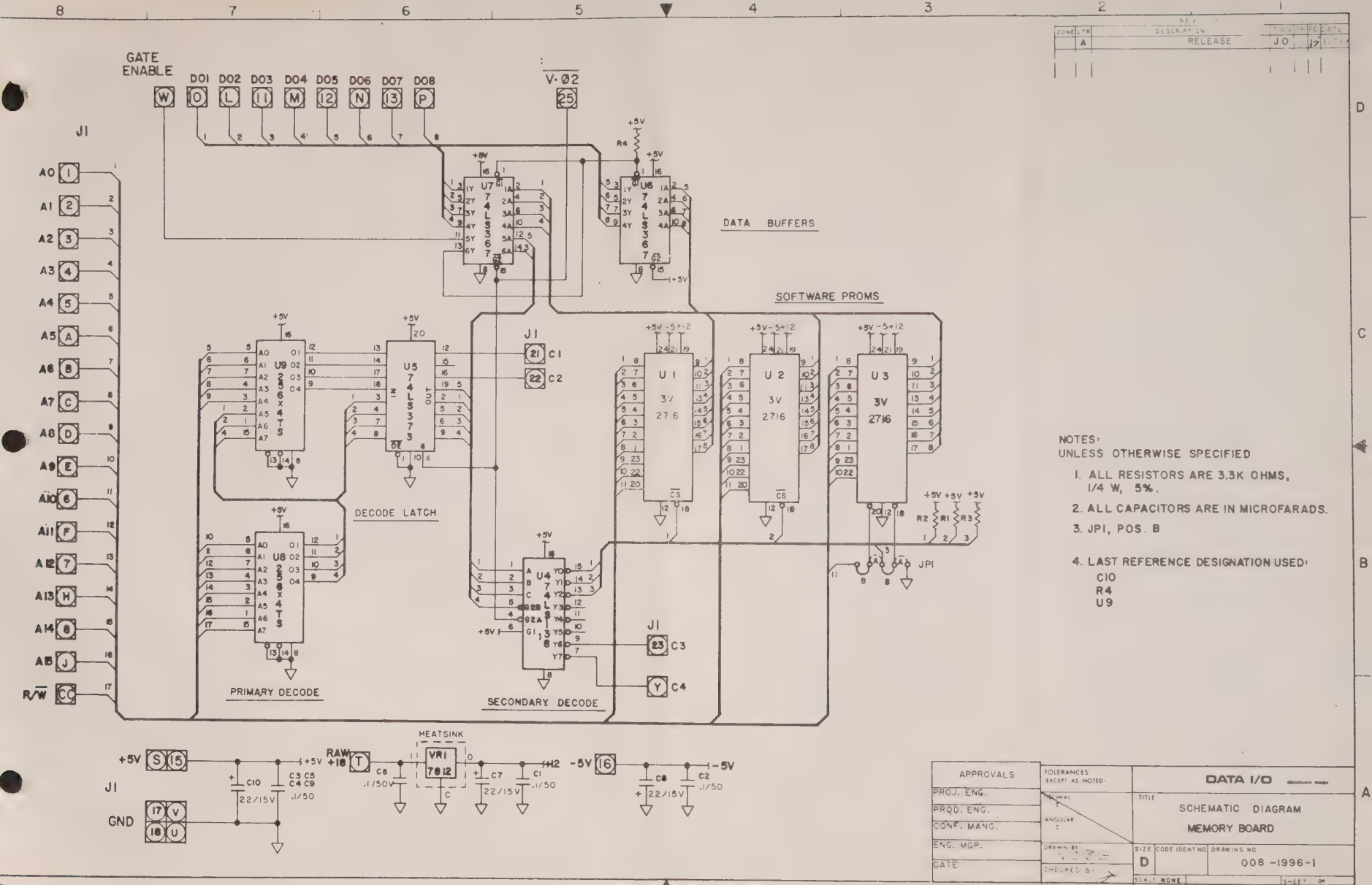
ACK	acknowledge
BEL	bell
BS	backspace
CAN	cancel
CR	carriage return
DC1	playback on, CNTL Q, X-ON
DC2	record on, CNTL R, PUNCH-ON, SOM
DC3	playback off, CNTL S, X-OFF
DC4	record off, CNTL T, PUNCH-OFF, EOM
DEL	delete, rubout
DLE	data link escape
EM	end of medium
ENQ	enquiry
EOT	end of transmission
ESC	escape
ETB	end of transmission block
ETX	end of text
FF	form feed
FS	file separater
GS	group separater
HT	horizontal tabulation
LF	line feed
NAK	negative acknowledge
NUL	null
RS	record separater
SI	shift in
SO	shift out
SOH	start of heading
STX	start of text
SUB	substitute
SYN	synchronous idle
US	unit separater
VT	vertical tab

APPENDIX C
SCHEMATICS

008-1542
008-1598
008-1996-1
008-1999


P1
OUTPUT REGS
OUTPUT SOURCE DRIVERS
U13
74LS377
U14
74LS377
U15
74LS244
DATA BUFFER
75453 (4 PLS)
8 = +5V
4 = GND
COMPARATORS
OUTPUT SINK DRIVERS
REF. GATE
LM339 (9 PLACES)
3 = +24
12 = GND
VP GEN
VFE SWITCH
VOP SWITCH
VOP GEN
VP SWITCH
OVERCURRENT MEM.
BACKWARDS DEVICE
VCC GEN
U1
723
J1 50 PIN
DATA I/O
SCHEMATIC DIAGRAM
SIGNETICS FPLF ANALOG NO. 1
008-1542
NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4W AND IN OHMS, ±5%.
2. ALL CAPACITORS ARE IN MICROFARADS.


REVISIONS
ZONE LTR DESCRIPTION DATE
A RELEASE 2/79
B ECN 3844 10-80
C ECN 3998 2/81
INPUT DRIVERS
DATA BUFFER
INPUT REG
P1
D0 9
DI 10
D2 11
D3 12
D4 13
D5 14
D6 15
D7 16
R/W 31
A0 1
A1 2
A2 3
A3 4
A4 5
A5 A
A6 B
A7 C
A8 D
A9 E
A10 6
A11 F
A12 7
A13 H
A14 8
A15 J
A02 32
GATE EN. JJ
EXT KK
U15 74LS245 10=GND 20=+5
U6 74LS377 REG A LOW 8820 10=GND 20=+5V
U7 74LS377 REG. C LOW 8860
U8 74LS377 REG A HIGH 88JF
U9 74LS377 REG C HIGH 885F
U1 75367 8=GND
U2 75367
U3 75367
U4 75367 8=GND
U5 75367
R21 100
C23 500PF
RP1 2.2K
RP2 2.2K
R1 2.2K
R2 2.2K
+PROG
R6 2.7 /2W
2N2907A Q3
R8 470
HEATSINK Q2 MJE800
R12 4.7K
R7 1K 1W
VIHH GEN
R3 470
R4 10K 5"
VR1 TL430
CR2 1N4148
C5 /50
CR1 1N4745A
OVERCURRENT MEMOPY
+5V
R14 4.7K
2N2907A Q7
2N2222 Q6
R10 4.7K
R13 510
R11 2K
CR4 1N4148
C27 .022
2N2484 Q4
R9 4.7K
C8 .022
74_S04
R16 2.2K
C9
SHORT R15 0K
Q5 2N2222
CE DRIVE.
C2 .01 /50V
R5 2.2K
+8V
HEATSINK
Q1 78-2 OUT COM
+12V
C7 /50V
CR3
50 PIN J1
10 33
I 32
12 31
13 30
14 29
15 28
16 27
17 26
18 1
19 2
110 3
111 4
112 5
113 6
114 7
115 8
CE (FOR CE) 12
9
16 THRU 20
35 THRU 39
44 THRU 50
GND
C1 C6 C13 C3 C10 C21 C4
+5V 21 +5V
C26 22/15
C25 .01
+PROG 22 +PROG
C12 .01
+18V LL +18V
C22 .1
-5V AA -5V
C24 22/15
GND DD 26 GND
CONFIG.
#1 13 17 VER A
C20 .1
#2 14 U VER B
C19 .1
#3 15 W 26
C11 .1
U13 PROM 2716 7000-7FFF +5=24 +12=19 -5=21 GND=12
U12 PROM 2716 7800-7FFF +5=24 +12=19 -5=21 GND=12 A10
U14 RAM 6810 8900-897F
U17 PROM 256X4 OC 8=GND 6=+5V
U16 PROM 32X8 OC 8=GND 16=+5V
100 (3PLCS)
500PF 3PLCS)
R17
R18
R20
C17 500PF
C18 500PF
RP4 3.3K
R19
3.3K RP4
RP3 4.0K
DECODE
U11 74LS32
74LS04
CLK BUFFER
OPERATE BB R22 1.2K
SENSE 24 R23
P1 29 DATA GATE SELECT
28 27 OUTPUT REG. SEL.
18 START
NN RR
MM PP
X
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. LAST REF DES USED: C27, R23, CR4, Q7
APPROVALS DATE
PROJ ENG 9/79
ENG MGR 11/79
NEXT ASSY
TOLERANCES DECIMALS ANGULAR X ± XX ± XXX ± DO NOT SCALE DRAWING
DRAWN BY T. CONNERTON 5/79
TITLE L. [illegible] 8/79
DATA I/O REDMOND, WASH.
TITLE SCHEMATIC DIAGRAM SIGNETICS FPLF ANALOG NO.2
SIZE D
CODE IDENT NO
DRAWING NO 008-1598
SCALE NONE
SHEET 1 OF 1

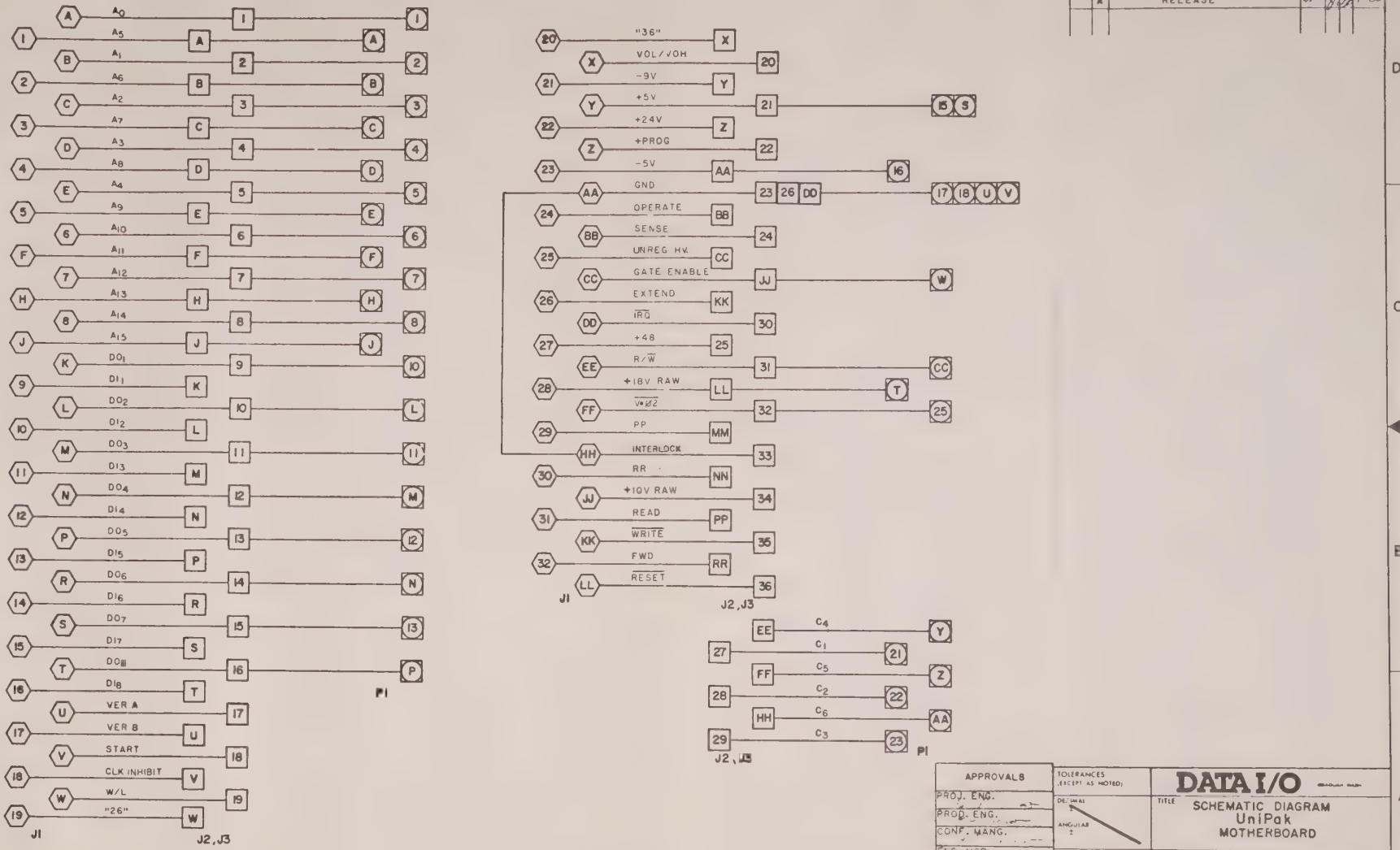


NOTES:
UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 3.3K OHMS, 1/4 W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. JPI, POS. B
4. LAST REFERENCE DESIGNATION USED:
   C10
   R4
   U9

ZONE	LTR	DESCRIPTION	DATE	APPD
	A	RELEASE	JO	

APPROVALS	TOLERANCES EXCEPT AS NOTED:	DATA I/O
PROJ. ENG.	DECIMAL ±	TITLE: SCHEMATIC DIAGRAM MEMORY BOARD
PROD. ENG.	ANGULAR ±	
CONF. MANG.		
ENG. MGR.	DRAWN BY	SIZE: D
DATE	CHECKED BY	CODE IDENT NO
	SCALE: NONE	DRAWING NO: 008-1996-1
		SHEET OF


REVISIONS
ZONE LTR DESCRIPTION DWN CK PE DATE
A RELEASE 1-80
A0 A5 A1 A6 A2 A7 A3 A8 A4 A9 A10 A11 A12 A13 A14 A15 DO1 DI1 DO2 DI2 DO3 DI3 DO4 DI4 DO5 DI5 DO6 DI6 DO7 DI7 DO8 DI8 VER A VER B START CLK INHIBIT W/L "26"
J1
J2, J3
"36" VOL/VOH -9V +5V +24V +PROG -5V GND OPERATE SENSE UNREG HV. GATE ENABLE EXTEND IRQ +48 R/W +18V RAW V•√2 PP INTERLOCK RR +10V RAW READ WRITE FWD RESET
J1
J2, J3
C4 C1 C5 C2 C6 C3
J2, J3
P1
APPROVALS
PROJ. ENG.
PROD. ENG.
CONF. MANG.
ENG. MGR.
DATE 1-17-80
TOLERANCES (EXCEPT AS NOTED)
DECIMAL
ANGULAR ±
DRAWN BY G. ENDER
CHECK
DATA I/O
TITLE SCHEMATIC DIAGRAM UniPak MOTHERBOARD
SIZE D
CODE IDENT NO
DRAWING NO 008-1999
SCALE NA
SHEET 1 OF 1

APPENDIX D
DATA ENTRY BY FUSE NUMBER

The programming module treats the IFL device as an addressable memory. Each IFL fuse is assigned a bit at a programmer data RAM address and fuses are selectively programmed using RAM data.

In some cases it may be necessary to examine the programming data fuse by fuse, or modify the data on a fuse by fuse basis. This can be accomplished using Select Function EE in the following manner:

1. Press SELECT, then EE.
2. Press ENTER or START.
3. The programmer will display a fuse number. Enter the fuse number that you want to examine or change (the fuse number must be in decimal form).
4. Press ENTER on the System 19. Press START on the 29A or 100A.
5. Enter 1 (program the fuse) or Ø (don't program the fuse). Press ENTER on the System 19, or START on the 29A or 100A. The fuse number will be incremented by one.
6. To enter a new fuse number on the System 19, press SELECT. On the 29A or 100A, go back to step 1.

To exit this mode, press KEYBD on the System 17 or 19. Press any function key on the 29A or 100A.

Each fuse in the IFL device is assigned a unique fuse number (refer to the Logic Diagrams). The data is stored in the programmer data RAM separately, starting from address Ø and bit Ø. To calculate the data RAM location for a particular fuse number:

1. Divide the fuse number by eight. For example,

$$\frac{1356}{8} = 169, \text{ remainder } 4$$

2. Convert the decimal quotient (169) to hexadecimal. 169 (decimal) = A9 (hexadecimal)
3. The hexadecimal quotient (A9 in the example) will give you the byte number.
4. The remainder (4 in the example) will give you the bit number. For example, address A9 contains fuse number 1352 through 1359.

BIT NUMBER (at address A9)	FUSE NUMBER
Ø	1352
1	1353
2	1354
3	1355
4	1356
5	1357
6	1358
7	1359

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_____

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